

RogueOne 13" Schematics Whiskey Lake-U

2018-07-09

REV : A00 (17925-1)

DELL

DY : None Installed
UMA: UMA only installed

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

RogueOne 13"

Rev

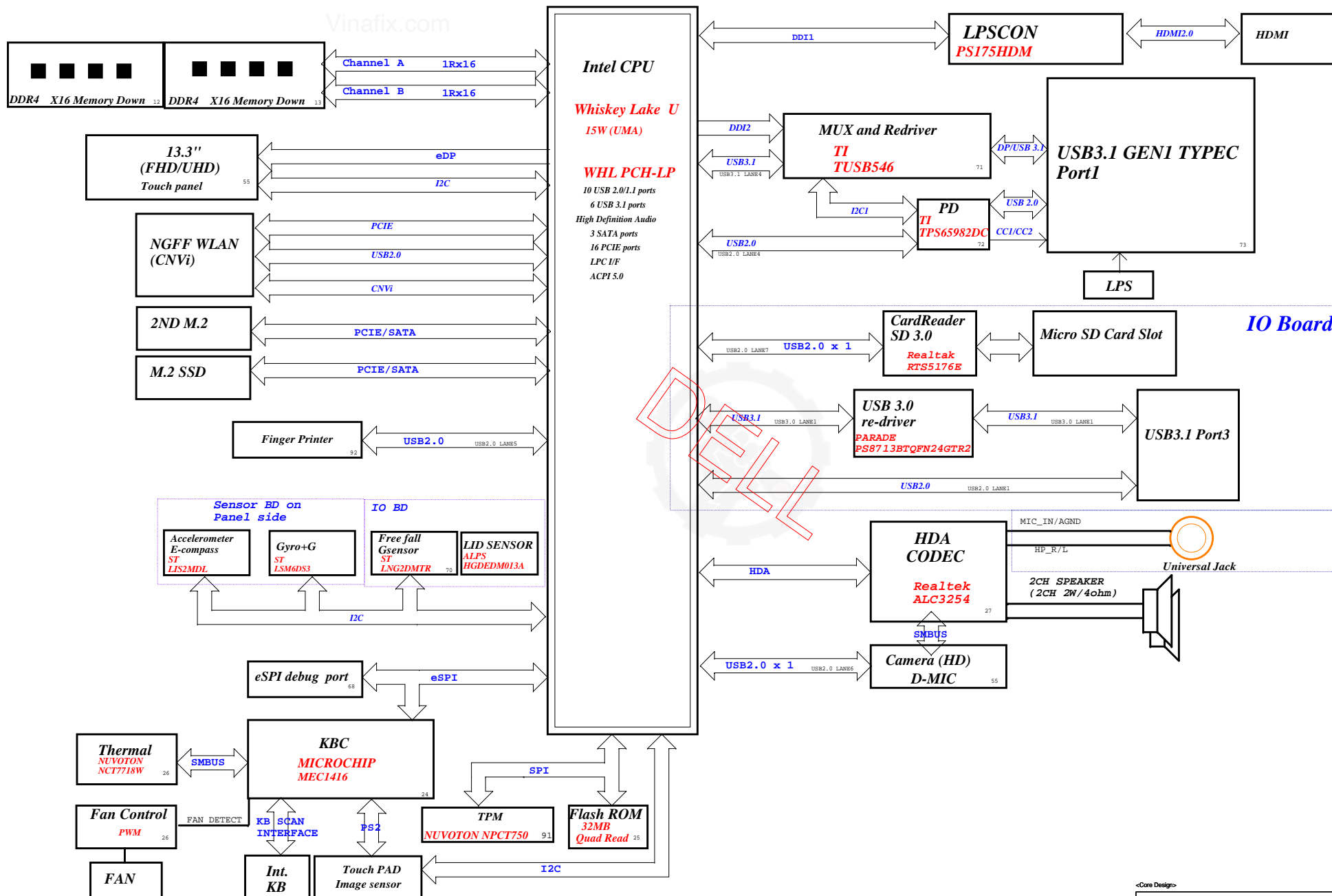
SC

Date: Thursday, August 02, 2018

Sheet 1 of 106

WHL-U 13" CPU 15W Block Diagram

Project code: 4PD0EZ010001
PCB P/N: 17925
Revision: -1



<Core Design>

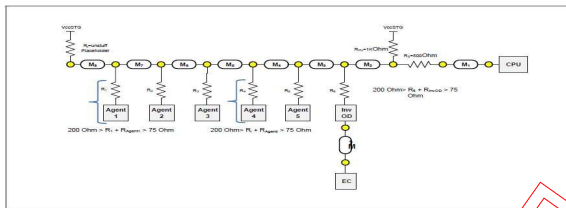
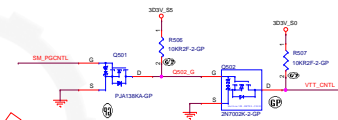
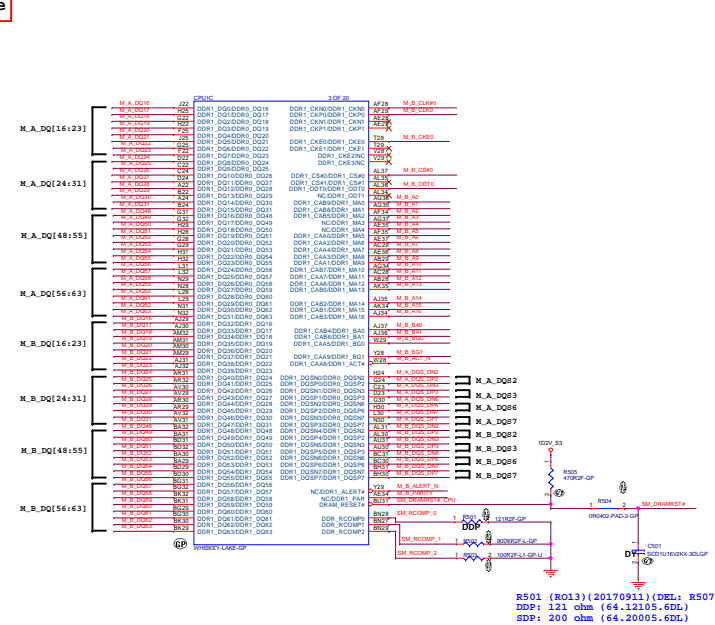
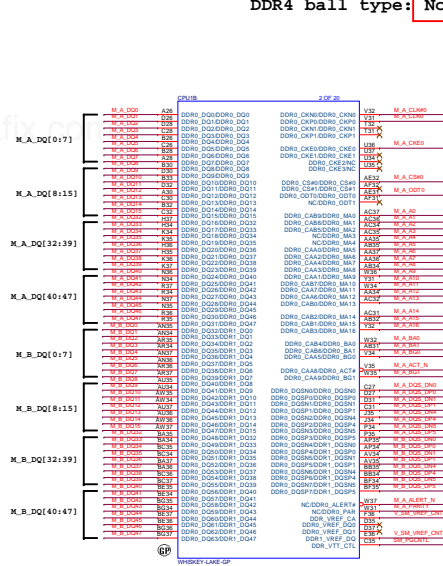
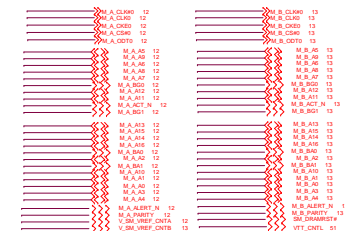
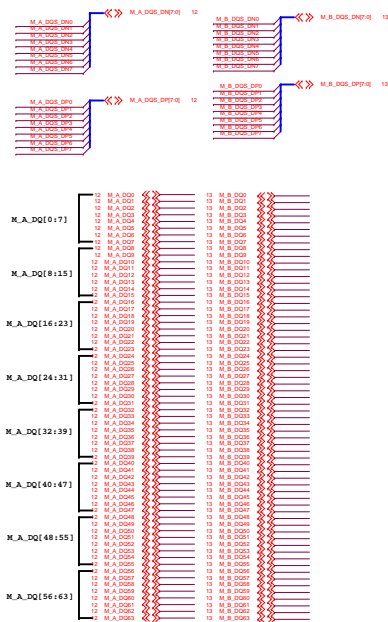


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1496.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values		Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω					
Platform resistors tolerances		± 5%					



Design Guideline:
SM_RCOMP keep routing length less than 500 mils

Table 4-8. WHL U DDR4 x16 Memory Down Routing Guideline (mils)

[illegible]

PDG: DDR/ODT

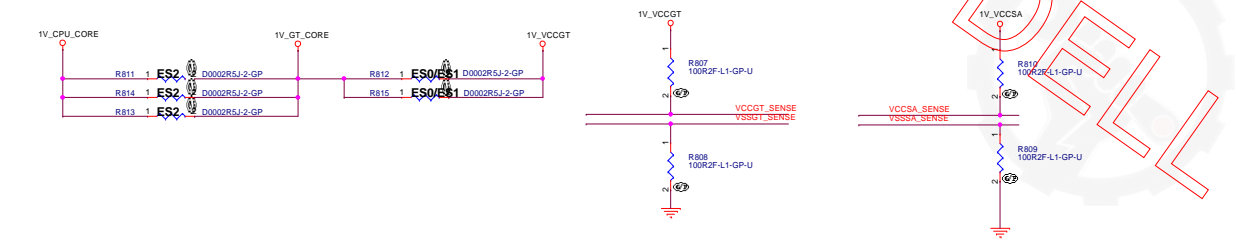
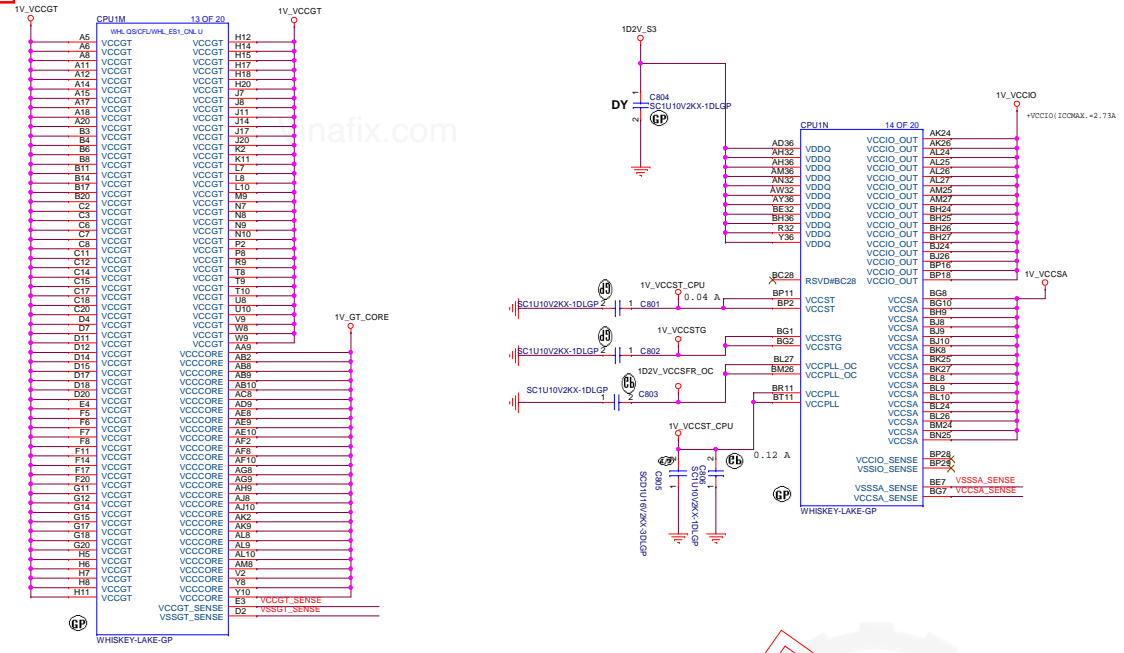
4.3 ODT Connectivity

Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	
Note: 1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.				

Note

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.




Pin Number	CFL-U43E	WHL E51 Netname	WHL E52 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

(Blanking)



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size
A3

Document Number
RogueOne 13"

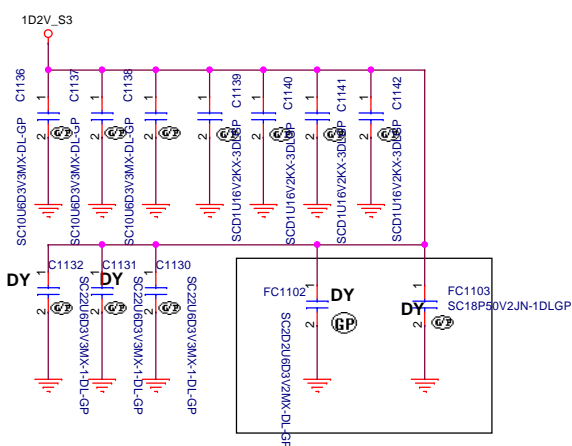
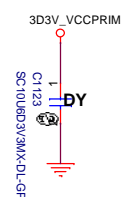
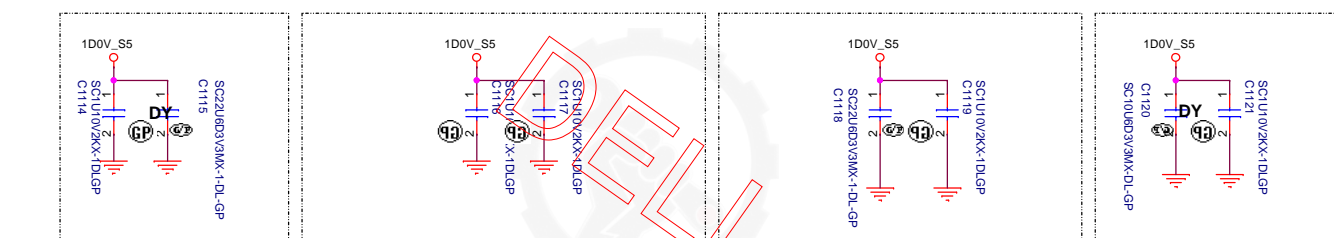
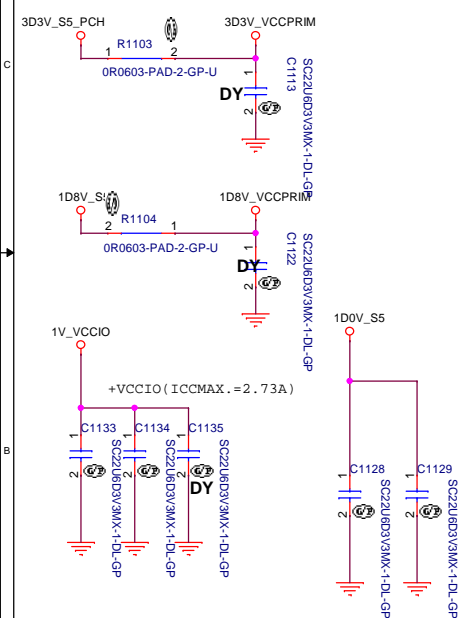
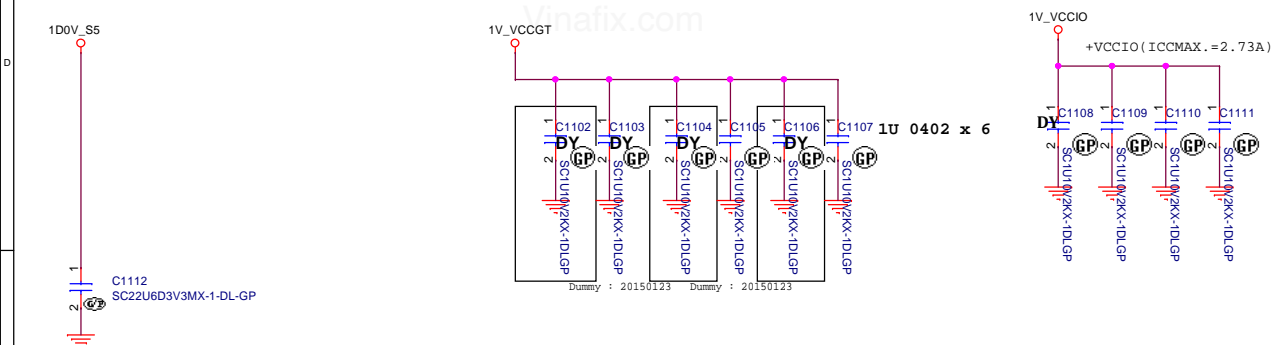
Rev
SC

Date: Thursday, August 02, 2018

Sheet 9 of 106

Main Func = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO

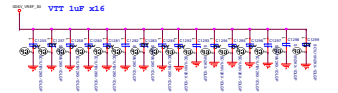
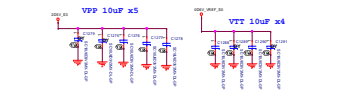
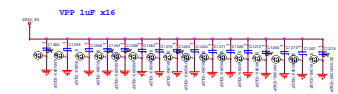
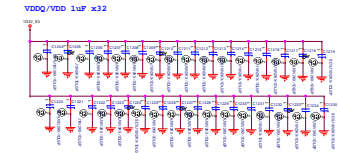
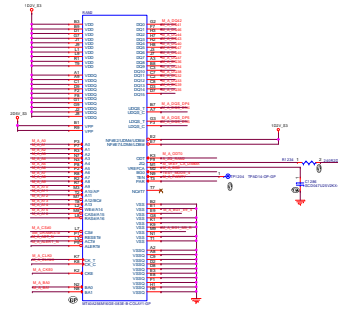
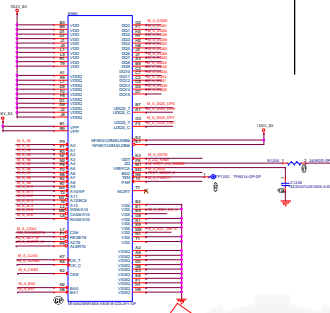
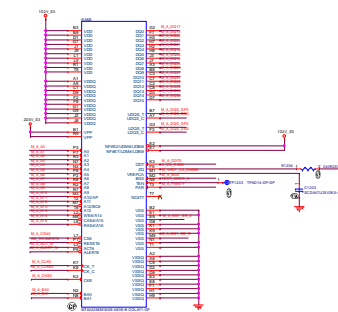
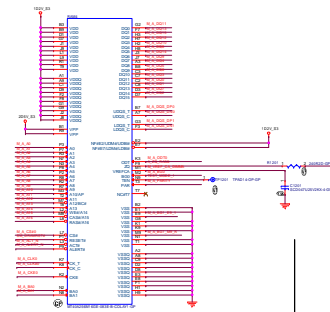
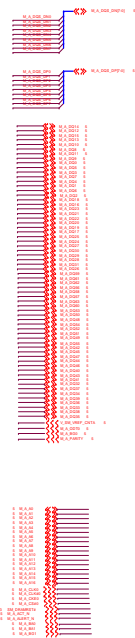


<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (Power CAP2)			
Size	Document Number	Rev	
A3	RogueOne 13"	SC	
Date:	Thursday, August 02, 2018	Sheet 11 of	106



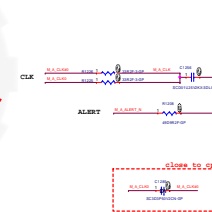
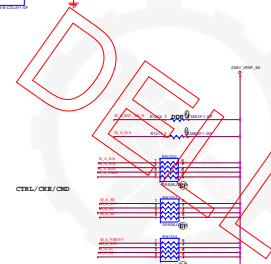
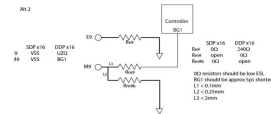
SDP & DDP SETTING

R1212-R1215 (R013)(20170911)(DEL: R1216-R1219)
SDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)



DDP x16 and SDP x16 Compatible Layout

- ▶ Alternate two layout, risk of VSS offset increases a little

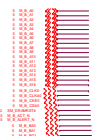
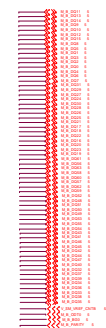


4.7.2 WHL-U DDR4 Memory Down Decoupling

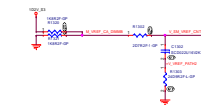
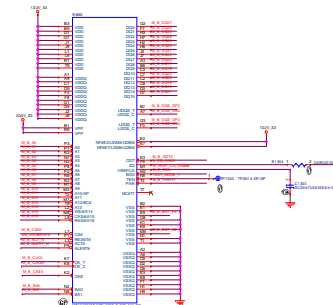
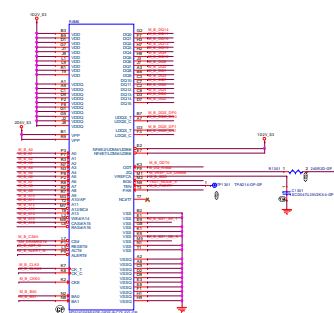
This recommendation assumes a 2Ch memory down implementation.

Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x uP (size)
DDR4 Memory Domain x16 - 4 Devices per Channel	VDDQ/VDD (shared)	4 per dram, as close as possible distribute evenly across domain, close by Drams	32x 1uF (0402) (All stuffed) 10x 15uF ¹ (0603) (All stuffed)
	VPP	2 per dram, as close as possible distribute evenly across domain, close by Drams	16x 1uF (0402) 5x 1uF (0603)
	VTT	distributed along termination resistors	16x 1uF (0402)
		distribute evenly across domain	4x 1uF (0603)



Vinafix.com

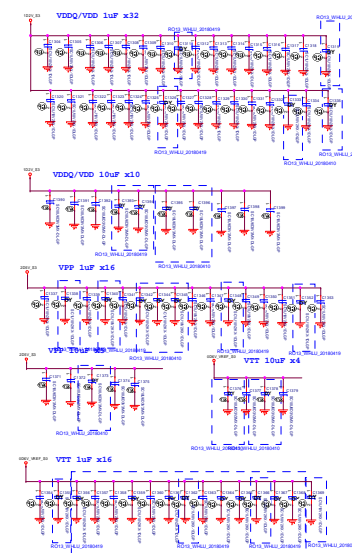


4.7.2 WHL-U DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

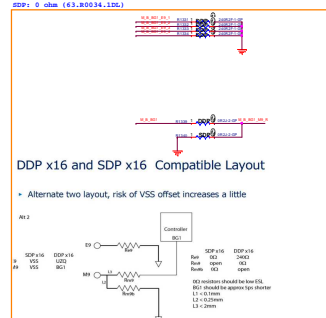
Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (nF)
DDR4 Memory Down x16 = 8 Banks per Channel	VDDQ/VDDQ (DQ/DQS)	4 per dram, as close as possible	32x 1uF (0402) (All stuffed)
		Distribute evenly across domain, close by Drams	150x 10uF (0603) (All stuffed)
	VPP	2 per dram, as close as possible	16x 1uF (0402)
	VTT	8 distribute evenly across domain, close by Drams	5x 10uF (0402) 16x 1uF (0402) Distribute evenly across domain



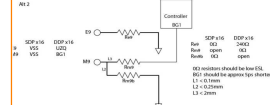
SDP & DDP SETTING

R1331-R1334 (R0L3) (20170911) (DRC: R1335-R1338)
SDP: 240 ohm (44-240015-0201)
DDP: 0 ohm (43-R0034-10C)

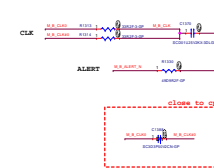
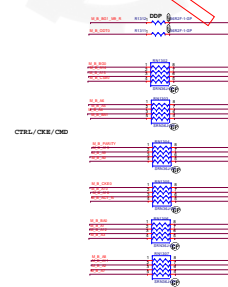


DDP x16 and SDP x16 Compatible Layout

- Alternate two layout, risk of VSS offset increases a little



CTRL/CLK/CLK



Vinafix.com

(Blanking)



<Core Design>

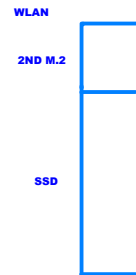
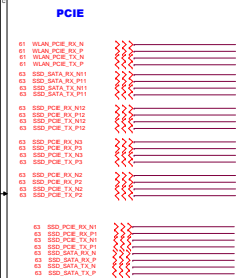
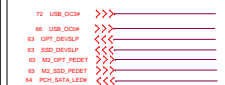
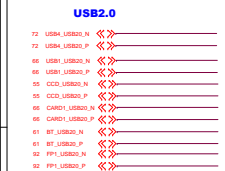


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM _SODIMM4

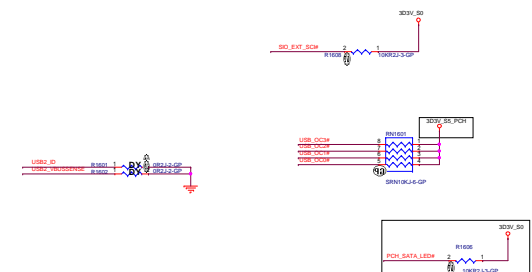
Size A4	Document Number RogueOne 13"	Rev SC
------------	--	------------------

Date: Thursday, August 02, 2018 Sheet 14 of 106



USB 2.0 Table

Pair	Device
1	USB3.0 Port1 (1080D)
2	N/A
3	N/A
4	Type-c
5	Fingerprint
6	CAMERA
7	Card Reader
8	N/A
9	N/A
10	MEAN (BT)



		USB2.0 (10 Ports)									
Premium / Base		USB2 #1	USB2 #2	USB2 #3	USB2 #4	USB2 #5	USB2 #6	USB2 #7	USB2 #8 (Frontview-U only)	USB2 #9 (Frontview-U only)	USB2 #10
CY8 Port Mapping	External Port (Type-C K)	External Port (Type-C K)	External Port (Type-C K)	External Port (Type-C K)	Fingerprint	Camera	Card Reader				BT
RD13_WHL	USB2.0 (Type-C K)			TYPE-C	Fingerprint	Camera					BT

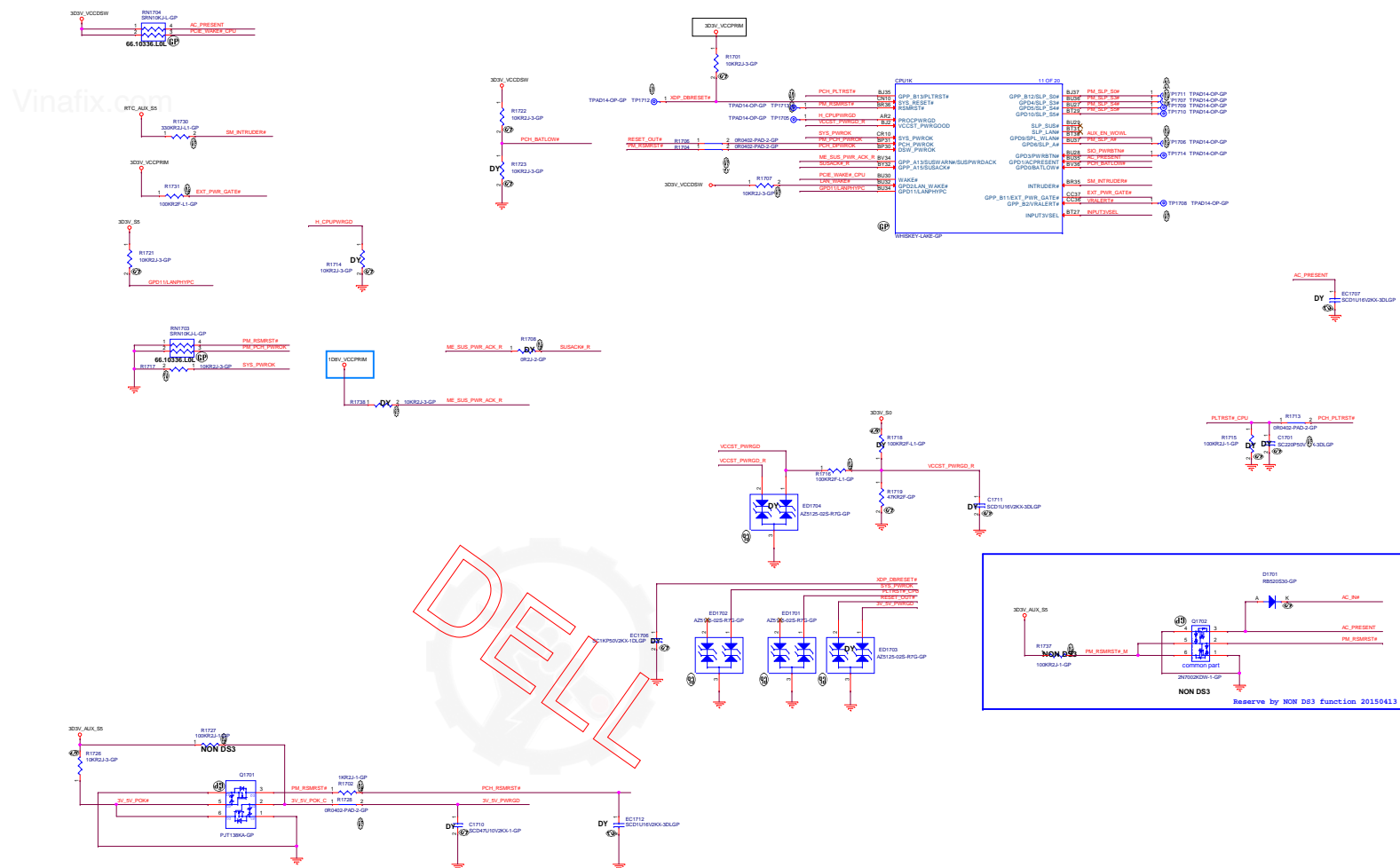
Premium / Base	PCI-X1														
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	00001 x1	00001 x2	00001 x3	00001 x4	00001 x5 (Premium 1000000)	00001 x6 (Premium 1000000)	00001 x7 (Premium 1000000)	00001 x8	00001 x9	00001 x10	00001 x11 (Premium 1000000)	00001 x12	00001 x13	00001 x14	00001 x15
	PCI-X1 x1	PCI-X1 x2	PCI-X1 x3	PCI-X1 x4	PCI-X1 x5	PCI-X1 x6	PCI-X1 x7	PCI-X1 x8	PCI-X1 x9	PCI-X1 x10	PCI-X1 x11	PCI-X1 x12	PCI-X1 x13	PCI-X1 x14	PCI-X1 x15
PCI-X4															
PCI-X4															
PCI-X4 (Intel RST for PCIe storage device R1)															
PCI-X4 (Intel RST for PCIe storage device R2)															
CPU	External Port Type/C1	External Port Type/C2	External Port Type/C3	External Port Type/C4	GPU (x4)		LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN
IO32_MHL	USB3.0 (IO board)	WWAN SSC	NA	TYPE-C	NA		NA	LAN	LAN	LAN	Optane (PCIe/SATA)	Optane (PCIe)	SSD (PCIe)	SSD (PCIe)	SSD (PCIe)

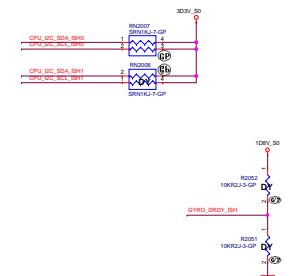
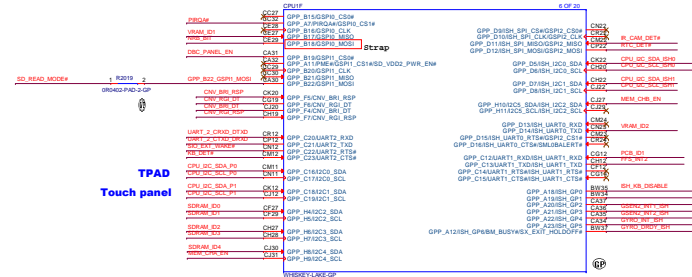
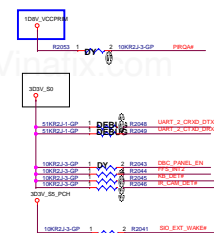
6.3 PCH PCI Express* Interface Design Guidelines

6.3.1 PCH PCI Express* Interface Configuration Details

Figure 6-2. Supported PCH PCI Express® Link Configurations

[illegible]

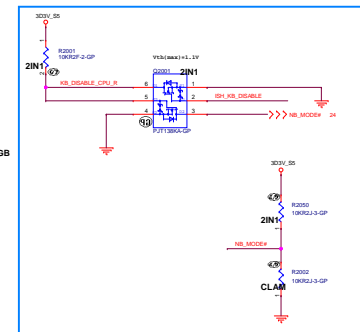
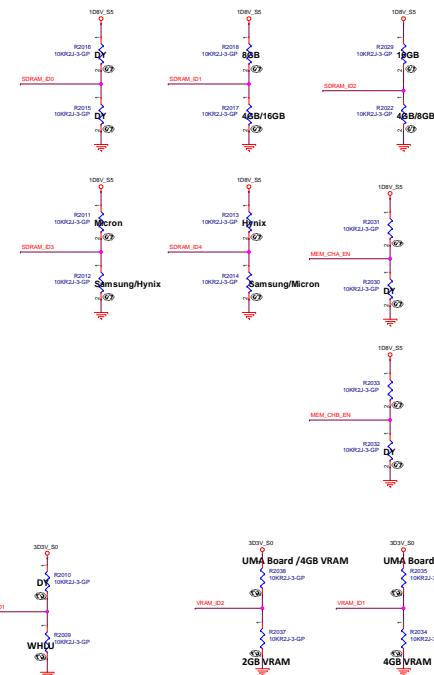




RAM ID

Vendor	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mfr. PN	Watson. P/N	Capacity
Samsuag	NA	01	00	K4AAG165WB-MCRC	TBD	16G
Micron	NA	01	10	MT40A1G16KNR-075R	TBD	16G
Hynix	NA	01	01	H5ANAG6NAMR-UHC	TBD	16G
Samsuag	NA	10	00	K4A8G165WB-MCRC	TBD	8G
Micron	NA	10	10	MT40A51M16LY-075R	TBD	8G
Hynix	NA	10	01	H5AN8G6NAPR-UHC	TBD	8G
Samsuag	NA	00	00	K4AAG165WB-MCRC	072.44165-0000	4G
Micron	NA	00	10	MT40A26M16GE-083B	072.40256-0000	4G
Hynix	NA	00	01	H5AN4G6NBJR-UHC	TBD	4G

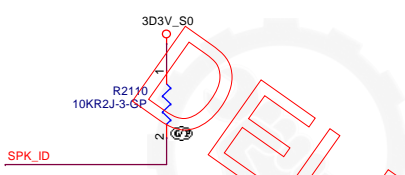
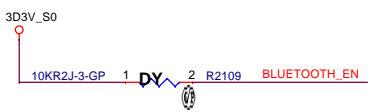
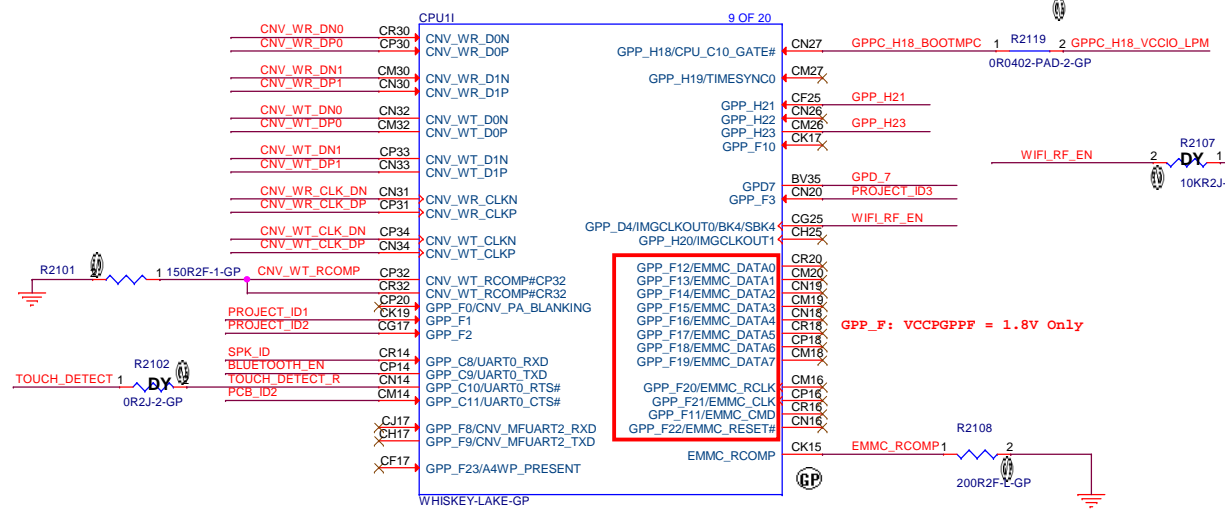
MEM_CONFIG[4:3]	On board memory config for chip vendor	11	DiMM Design
		10	Hylix
		01	Micron
		00	Samsung
MEM_CONFIG[2:1]	On board memory config for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	Reserved (non-use)		



Main Func = PCH

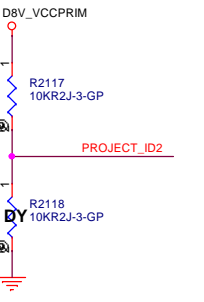
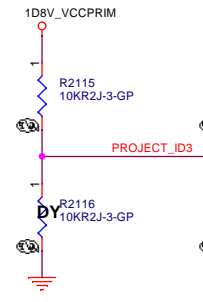
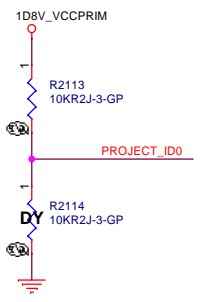
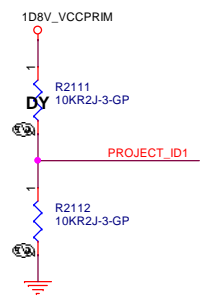
- 61 WIFI_RF_EN <<<
- 29 SPK_ID >>>
- 61 BLUETOOTH_EN <<<
- 55 TOUCH_DETECT <<<
- 20 PCB_ID2 <<<
- 15 GPP_H21 <<<
- 15 GPP_H23 <<<
- 15 GPD_7 <<<
- 61 CNV_WT_CLK_DP >>>
- 61 CNV_WT_CLK_DN >>>
- 61 CNV_WT_DP0 >>>
- 61 CNV_WT_DN0 >>>
- 61 CNV_WT_DP1 >>>
- 61 CNV_WT_DN1 >>>
- 61 CNV_WR_CLK_DP >>>
- 61 CNV_WR_CLK_DN >>>
- 61 CNV_WR_DP0 >>>
- 61 CNV_WR_DN0 >>>
- 61 CNV_WR_DP1 >>>
- 61 CNV_WR_DN1 >>>
- 40 GPPC_H18_VCCIO_LPM <<<
- 18 PROJECT_ID0 <<<

Vinafix.com



PROJECT_ID[1:0] 01: 7000 Series

PROJECT_ID[3:2] 11: Inspiron



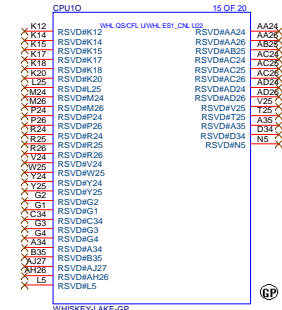
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (EMMC/CNVi)**

Size A3	Document Number	Rev SC
Date: Thursday, August 02, 2018		Sheet 21 of 106

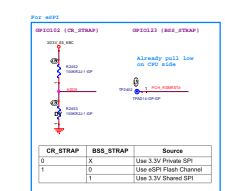
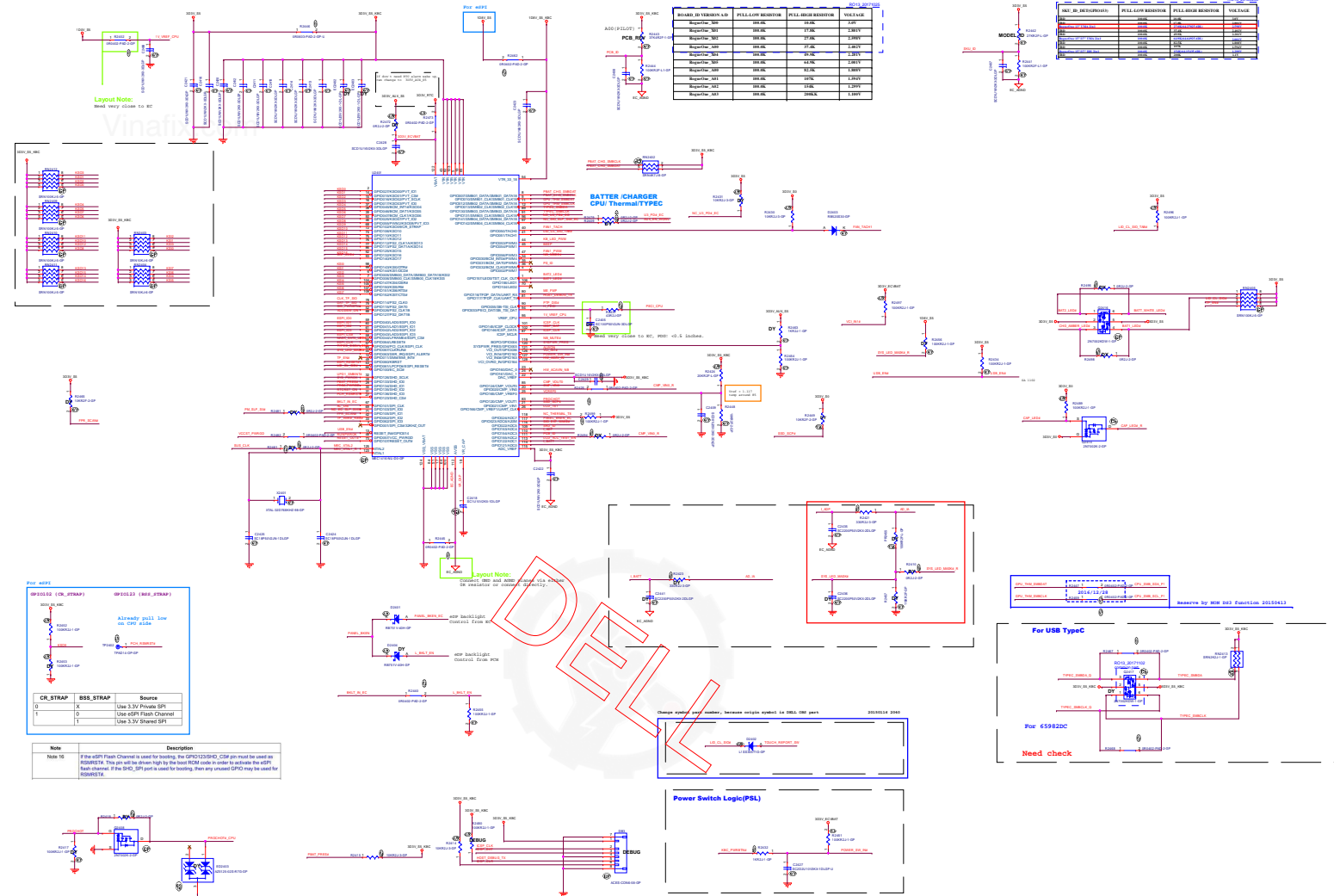
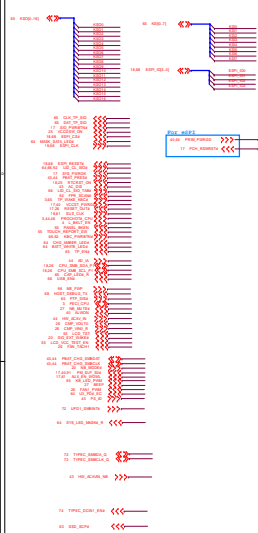
Main Func = PCH



CPU1R 18 OF 20		
CR34	VSS	BL7
BT5	VSS	AL35
BY5	VSS	BT36
CP35	VSS	AL35
CM37	VSS	CM5
AW1	VSS	AE27
CM1	VSS	BM65
BD6	VSS	CM9
AV4	VSS	AE39
BS4	VSS	AE7
E35	VSS	BM9
AE24	VSS	AF27
AE36	VSS	BM15
AF25	VSS	CH21
AG24	VSS	AF3
AC25	VSS	E33
AH24	VSS	CH25
AF25	VSS	AP30
B2	VSS	CN29
B36	VSS	AF33
C36	VSS	BP15
C37	VSS	AF36
CN1	VSS	AF4
CN2	VSS	CN5
CN37	VSS	AF7
CP2	VSS	BP25
D1	VSS	CH9
A32	VSS	AG10
F33	VSS	BP3
A3	VSS	CP1
BL7	VSS	BP32
A36	VSS	CP11
BR10	VSS	AN6
CL4	VSS	BP33
AB27	VSS	AP15
BK2	VSS	AP18
CK1	VSS	AP19
AB3	VSS	AP20
BK29	VSS	AP21
AB30	VSS	AP22
BK3	VSS	AP23
CK4	VSS	AP24
AB33	VSS	AP25
BK33	VSS	AP26
CK7	VSS	AP27
AB36	VSS	AP28
BK4	VSS	AP29
CL2	VSS	AP30
A4	VSS	AP31
BK7	VSS	AP32
CM13	VSS	AP33
AB7	VSS	AP34
BL25	VSS	AP35
CM17	VSS	AP36
AC10	VSS	AP37
CM21	VSS	AP38
BL28	VSS	AP39
CM27	VSS	AP40
BL29	VSS	AP41
CM25	VSS	AP42
AC30	VSS	AP43
BL30	VSS	AP44
CM29	VSS	AP45
BL31	VSS	AP46
CM31	VSS	AP47
AL33	VSS	AP48
BL32	VSS	AP49
CM33	VSS	AP50
AD35	VSS	AP51

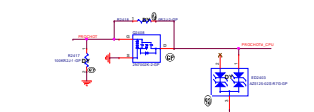
CPU1S 19 OF 20		
BT35	VSS	BY25
D6	VSS	J18
AL35	VSS	AL32
BT36	VSS	BY28
D6	VSS	BT31
AL7	VSS	CM5
D6	VSS	AE27
AM10	VSS	BM65
BU11	VSS	CM9
E23	VSS	AE39
AM29	VSS	CM9
E27	VSS	AE7
AM33	VSS	BM9
BU23	VSS	AF27
E27	VSS	BM15
AM35	VSS	CH21
BU24	VSS	AF3
E33	VSS	E33
AN25	VSS	CH25
BU27	VSS	AP30
E33	VSS	CN29
AN29	VSS	AF33
BU11	VSS	BP15
F12	VSS	AF36
AN29	VSS	AF4
F15	VSS	CN5
AN30	VSS	AF7
F15	VSS	BP25
AN31	VSS	CH9
BY3	VSS	AG10
F2	VSS	BP3
AN7	VSS	CP1
BY17	VSS	BP32
F21	VSS	CP11
BY33	VSS	AN6
F24	VSS	BP33
BY4	VSS	AP15
F3	VSS	AP18
BY11	VSS	AP19
AP3	VSS	AP20
BY15	VSS	AP21
G21	VSS	AP22
AP36	VSS	AP23
G27	VSS	AP24
AP4	VSS	AP25
G33	VSS	AP26
AP23	VSS	AP27
G36	VSS	AP28
Q39	VSS	AP29
AT33	VSS	AP30
AT35	VSS	AP31
AT36	VSS	AP32
H21	VSS	AP33
AT45	VSS	AP34
BW7	VSS	AP35
H27	VSS	AP36
AT4	VSS	AP37
BY11	VSS	AP38
BY15	VSS	AP39
H9	VSS	AP40
AU28	VSS	AP41
BY23	VSS	AP42
J12	VSS	AP43
AU29	VSS	AP44
J15	VSS	AP45
AL29	VSS	AP46

CPU1T 20 OF 20		
N6	VSS	CF23
BY7	VSS	V4
CE3	VSS	BE30
P10	VSS	CF28
BC	VSS	W10
CB33	VSS	BE31
P3	VSS	CF31
B7	VSS	W27
CE4	VSS	CF4
P33	VSS	W30
B9	VSS	BF3
CE7	VSS	CC33
P36	VSS	W7
BA10	VSS	BF33
CC11	VSS	CG7
P4	VSS	BF36
BD38	VSS	W26
P7	VSS	BF4
BA3	VSS	CH31
CC20	VSS	Y27
R27	VSS	Y30
BE3	VSS	CG25
CC25	VSS	CG28
R25	VSS	CJ11
BB33	VSS	Y33
CC28	VSS	CJ14
R29	VSS	Y36
BB36	VSS	BH28
CC31	VSS	CJ19
R30	VSS	Y7
BB4	VSS	BH29
CC4	VSS	CC23
R31	VSS	BH32
CC25	VSS	CJ28
CD11	VSS	BH33
AW31	VSS	CJ33
T27	VSS	BH36
CD12	VSS	CJ35
T30	VSS	BP19
CC29	VSS	BY19
CD14	VSS	BY19
T33	VSS	CC16
AW31	VSS	BL16
CA15	VSS	CC14
K30	VSS	BR22
CC22	VSS	T7
CC25	VSS	BU20
K31	VSS	CD20
AY36	VSS	BT14
K32	VSS	BP12
CE33	VSS	CB23
U26	VSS	CC24
BD3	VSS	U7
CE35	VSS	U2
U7	VSS	U2
BD33	VSS	U2
CE36	VSS	U2
U29	VSS	AK4
BD35	VSS	AU4
CE7	VSS	AW4
CE7	VSS	B46
BD36	VSS	BC4
CF11	VSS	BE4
V3	VSS	BE8
BD37	VSS	BD4
BE9	VSS	BD4
CF19	VSS	CJ3
BE9	VSS	AM5
CF2	VSS	AC5
BE3	VSS	AC5
CF2	VSS	CR6



CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use 65V Flash Channel
1	1	Use 3.3V Shared SPI

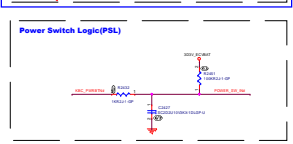
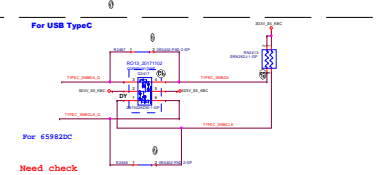
Note: If the vSPI Flash Channel is used for booting, the vSPI pin must be used as the boot channel. If the vSPI pin is used for booting, then any unused vSPI pins may be used for other functions.



Regulator	IN	OUT	TYPE
Regulator_100	100.00	1.00	1.00V
Regulator_101	100.00	1.00	1.00V
Regulator_102	100.00	1.00	1.00V
Regulator_103	100.00	1.00	1.00V
Regulator_104	100.00	1.00	1.00V
Regulator_105	100.00	1.00	1.00V
Regulator_106	100.00	1.00	1.00V
Regulator_107	100.00	1.00	1.00V

Regulator	IN	OUT	TYPE
Regulator_108	100.00	1.00	1.00V
Regulator_109	100.00	1.00	1.00V
Regulator_110	100.00	1.00	1.00V
Regulator_111	100.00	1.00	1.00V
Regulator_112	100.00	1.00	1.00V
Regulator_113	100.00	1.00	1.00V
Regulator_114	100.00	1.00	1.00V
Regulator_115	100.00	1.00	1.00V

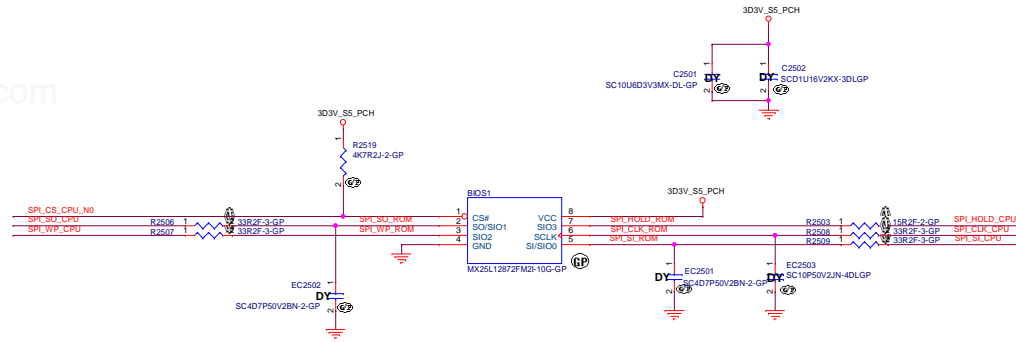
Reserve for NVR Del Equation 20150413



Main Func = SPI Flash

15,18 SPI_HOLD_CPU
18,91 SPI_CLK_CPU
15,18,91 SPI_SL_CPU
18 SPI_CS_CPU_N0
18,91 SPI_SO_CPU
15,18 SPI_WP_CPU

Vinafix.com



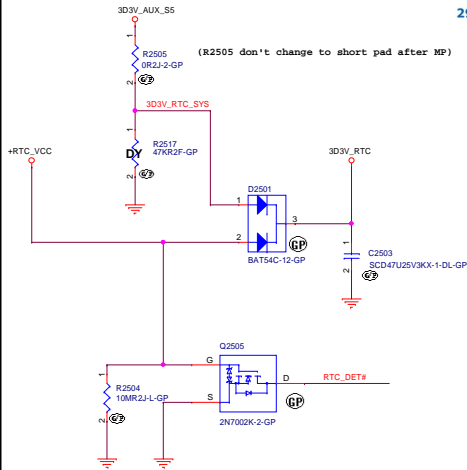
Main Func = RTC

18,24 RTCRST_ON
17,40,45 3V_SV_PWRGD
24 VCCDSW_ON
15,20 RTC_DET#
52,54 3V_SV_DSW_OK

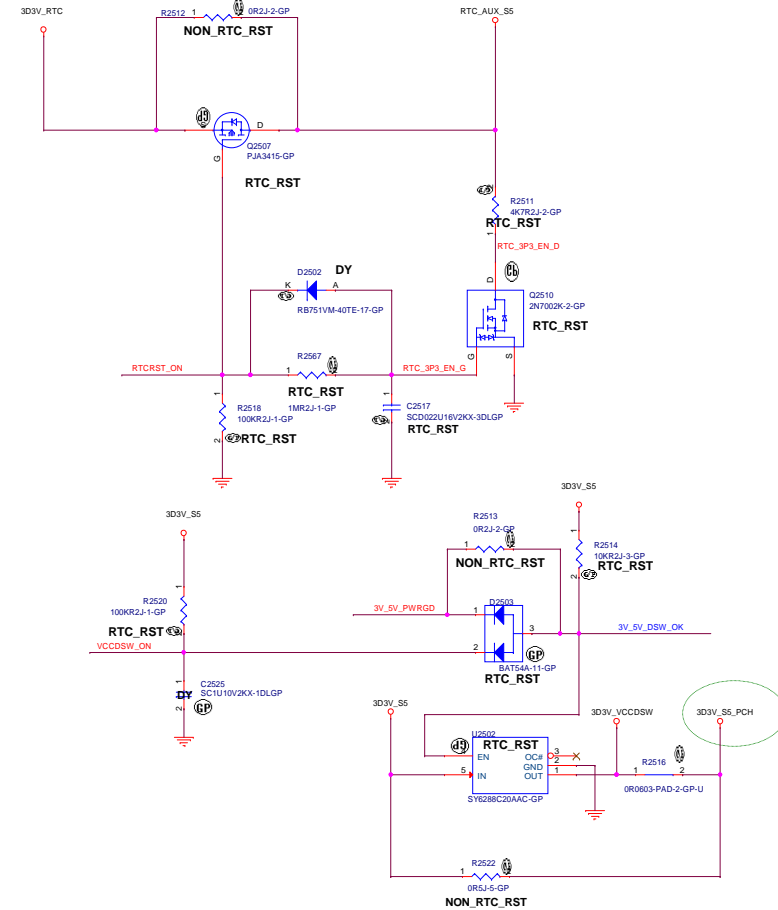
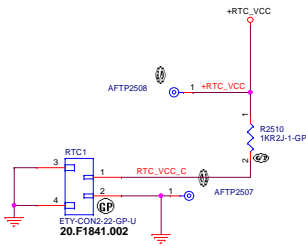
Delivery Voltage 3.19V

29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



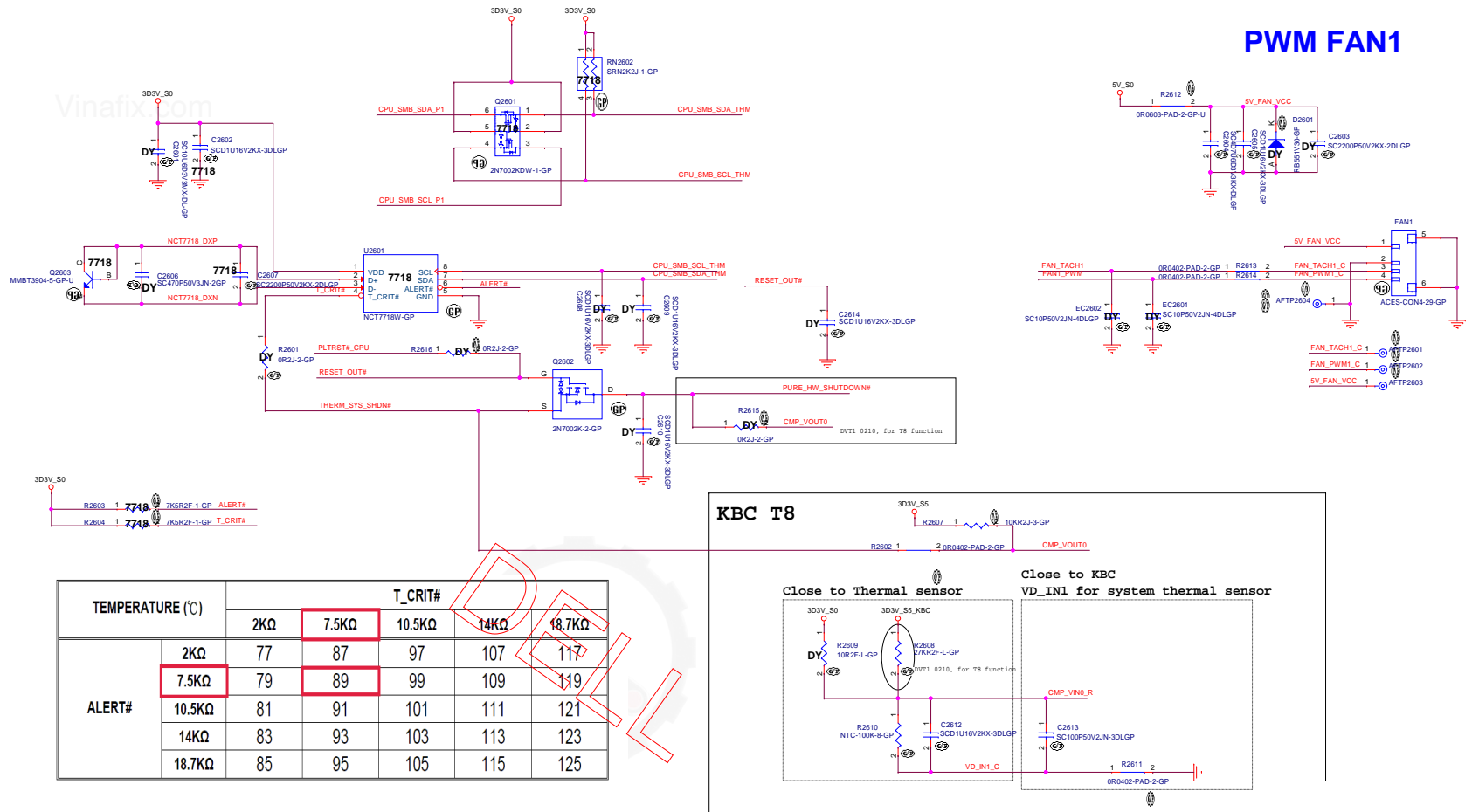
RTC



«Core Design»

Main Func = Thermal Sensor

- 18,24 CPU_SMB_SDA_PX
- 18,24 CPU_SMB_SCL_PX
- 17,61,63,91 PLTRSTV_CPU
- 17,24 RESET_OUT#
- 40 PURE_HW_SHUTDOWN#
- 24 FAN1_PWM
- 24 CMP_VOUT0
- 24 CMP_VIN0_R



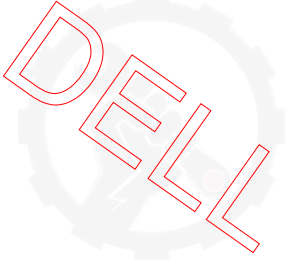
(Blanking)



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 28 of	106

(Blanking)



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 30 of	106

(Blanking)




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN RTL8106			
Size	Document Number		Rev
A4	RogueOne 13"		SC
Date: Thursday, August 02, 2018		Sheet 31 of	106

(Blanking)




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
XFOM&RJ45			
Size	Document Number		Rev
A4	RogueOne 13"		SC
Date: Thursday, August 02, 2018		Sheet 32 of	106

(Blanking)



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Card Reader-RTS5170			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 33 of	106

Vinafix.com




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A3	RogueOne 13"		SC
Date:	Thursday, August 02, 2018		Sheet 34 of 106

Vinafix.com



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB switch

Size	Document Number	Rev
	RogueOne 13"	SC

Date: Thursday, August 02, 2018	Sheet 35 of 106
---------------------------------	-----------------

Vinafix.com




<Core Design>


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB30			
Size	Document Number		Rev
A3	RogueOne 13"		SC
Date:	Thursday, August 02, 2018		Sheet 36 of 106

Vinafix.com



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A3	RogueOne 13"		SC
Date: Thursday, August 02, 2018		Sheet 37 of	106



(Blanking)



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 39 of	106



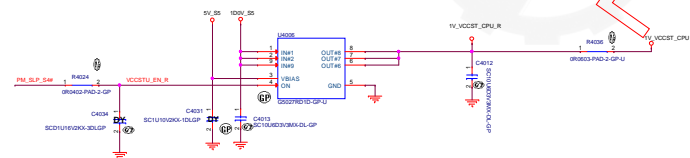
5V_S0

5V_S0 Consumption
Peak current 5A

3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

[illegible]

[#543016] Optional. Added for addition system robustness [source](#)


The schematic diagram illustrates the internal circuitry of the 074.05027 0093 component. It features a 100V_B3 input at the top, which is connected to a network of capacitors (C4006, C4007, C4008) and resistors (R4001, R4002, R4003, R4004, R4005, R4006, R4007, R4008, R4009, R4010, R4011, R4012, R4013, R4014, R4015, R4016, R4017, R4018, R4019, R4020, R4021, R4022, R4023, R4024, R4025, R4026, R4027, R4028, R4029, R4030, R4031, R4032, R4033, R4034, R4035, R4036, R4037, R4038, R4039, R4040, R4041, R4042, R4043, R4044, R4045, R4046, R4047, R4048, R4049, R4050, R4051, R4052, R4053, R4054, R4055, R4056, R4057, R4058, R4059, R4060, R4061, R4062, R4063, R4064, R4065, R4066, R4067, R4068, R4069, R4070, R4071, R4072, R4073, R4074, R4075, R4076, R4077, R4078, R4079, R4080, R4081, R4082, R4083, R4084, R4085, R4086, R4087, R4088, R4089, R4090, R4091, R4092, R4093, R4094, R4095, R4096, R4097, R4098, R4099, R4100, R4101, R4102, R4103, R4104, R4105, R4106, R4107, R4108, R4109, R4110, R4111, R4112, R4113, R4114, R4115, R4116, R4117, R4118, R4119, R4120, R4121, R4122, R4123, R4124, R4125, R4126, R4127, R4128, R4129, R4130, R4131, R4132, R4133, R4134, R4135, R4136, R4137, R4138, R4139, R4140, R4141, R4142, R4143, R4144, R4145, R4146, R4147, R4148, R4149, R4150, R4151, R4152, R4153, R4154, R4155, R4156, R4157, R4158, R4159, R4160, R4161, R4162, R4163, R4164, R4165, R4166, R4167, R4168, R4169, R4170, R4171, R4172, R4173, R4174, R4175, R4176, R4177, R4178, R4179, R4180, R4181, R4182, R4183, R4184, R4185, R4186, R4187, R4188, R4189, R4190, R4191, R4192, R4193, R4194, R4195, R4196, R4197, R4198, R4199, R4200, R4201, R4202, R4203, R4204, R4205, R4206, R4207, R4208, R4209, R4210, R4211, R4212, R4213, R4214, R4215, R4216, R4217, R4218, R4219, R4220, R4221, R4222, R4223, R4224, R4225, R4226, R4227, R4228, R4229, R4230, R4231, R4232, R4233, R4234, R4235, R4236, R4237, R4238, R4239, R4240, R4241, R4242, R4243, R4244, R4245, R4246, R4247, R4248, R4249, R4250, R4251, R4252, R4253, R4254, R4255, R4256, R4257, R4258, R4259, R4260, R4261, R4262, R4263, R4264, R4265, R4266, R4267, R4268, R4269, R4270, R4271, R4272, R4273, R4274, R4275, R4276, R4277, R4278, R4279, R4280, R4281, R4282, R4283, R4284, R4285, R4286, R4287, R4288, R4289, R4290, R4291, R4292, R4293, R4294, R4295, R4296, R4297, R4298, R4299, R4300, R4301, R4302, R4303, R4304, R4305, R4306, R4307, R4308, R4309, R4310, R4311, R4312, R4313, R4314, R4315, R4316, R4317, R4318, R4319, R4320, R4321, R4322, R4323, R4324, R4325, R4326, R4327, R4328, R4329, R4330, R4331, R4332, R4333, R4334, R4335, R4336, R4337, R4338, R4339, R4340, R4341, R4342, R4343, R4344, R4345, R4346, R4347, R4348, R4349, R4350, R4351, R4352, R4353, R4354, R4355, R4356, R4357, R4358, R4359, R4360, R4361, R4362, R4363, R4364, R4365, R4366, R4367, R4368, R4369, R4370, R4371, R4372, R4373, R4374, R4375, R4376, R4377, R4378, R4379, R4380, R4381, R4382, R4383, R4384, R4385, R4386, R4387, R4388, R4389, R4390, R4391, R4392, R4393, R4394, R4395, R4396, R4397, R4398, R4399, R4400, R4401, R4402, R4403, R4404, R4405, R4406, R4407, R4408, R4409, R4410, R4411, R4412, R4413, R4414, R4415, R4416, R4417, R4418, R4419, R4420, R4421, R4422, R4423, R4424, R4425, R4426, R4427, R4428, R4429, R4430, R4431, R4432, R4433, R4434, R4435, R4436, R4437, R4438, R4439, R4440, R4441, R4442, R4443, R4444, R4445, R4446, R4447, R4448, R4449, R4450, R4451, R4452, R4453, R4454, R4455, R4456, R4457, R4458, R4459, R4460, R4461, R4462, R4463, R4464, R4465, R4466, R4467, R4468, R4469, R4470, R4471, R4472, R4473, R4474, R4475, R4476, R4477, R4478, R4479, R4480, R4481, R4482, R4483, R4484, R4485, R4486, R4487, R4488, R4489, R4490, R4491, R4492, R4493, R4494, R4495, R4496, R4497, R4498, R4499, R4500, R4501, R4502, R4503, R4504, R4505, R4506, R4507, R4508, R4509, R4510, R4511, R4512, R4513, R4514, R4515, R4516, R4517, R4518, R4519, R4520, R4521, R4522, R4523, R4524, R4525, R4526, R4527, R4528, R4529, R4530, R4531, R4532, R4533, R4534, R4535, R4536, R4537, R4538, R4539, R4540, R4541, R4542, R4543, R4544, R4545, R4546, R4547, R4548, R4549, R4550, R4551, R4552, R4553, R4554, R4555, R4556, R4557, R4558, R4559, R4560, R4561, R4562, R4563, R4564, R4565, R4566, R4567, R4568, R4569, R4570, R4571, R4572, R4573, R4574, R4575, R4576, R4577, R4578, R4579, R4580, R4581, R4582, R4583, R4584, R4585, R4586, R4587, R4588, R4589, R4590, R4591, R4592, R4593, R4594, R4595, R4596, R4597, R4598, R4599, R4600, R4601, R4602, R4603, R4604, R4605, R4606, R4607, R4608, R4609, R4610, R4611, R4612, R4613, R4614, R4615, R4616, R4617, R4618, R4619, R4620, R4621, R4622, R4623, R4624, R4625, R4626, R4627, R4628, R4629, R4630, R4631, R4632, R4633, R4634, R4635, R4636, R4637, R4638, R4639, R4640, R4641, R4642, R4643, R4644, R4645, R4646, R4647, R4648, R4649, R4650, R4651, R4652, R4653, R

The diagram shows a 150mA current source circuit. It features a 2N964A JFET with its gate connected to a 100k resistor (R4024) and its source connected to a 200k resistor (R4035). The drain is connected to a 100k resistor (R4023) and a 100VDC-10A supply. The source is connected to a 200VDC-1A supply. The output current is 150mA.

Vinafix.com



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Connected_Standby(1/2)+DS3		
Size A4	Document Number RogueOne 13"	Rev SC
Date: Thursday, August 02, 2018		Sheet 41 of 106

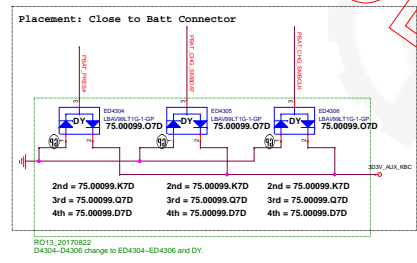
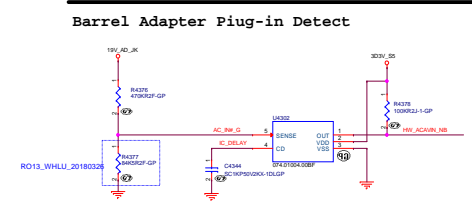
(Blanking)

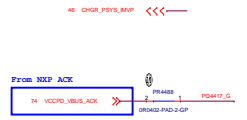
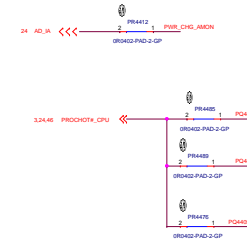
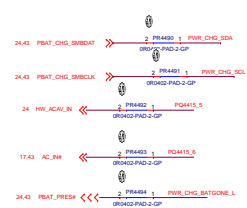


<Core Design>

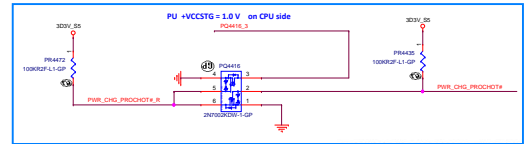
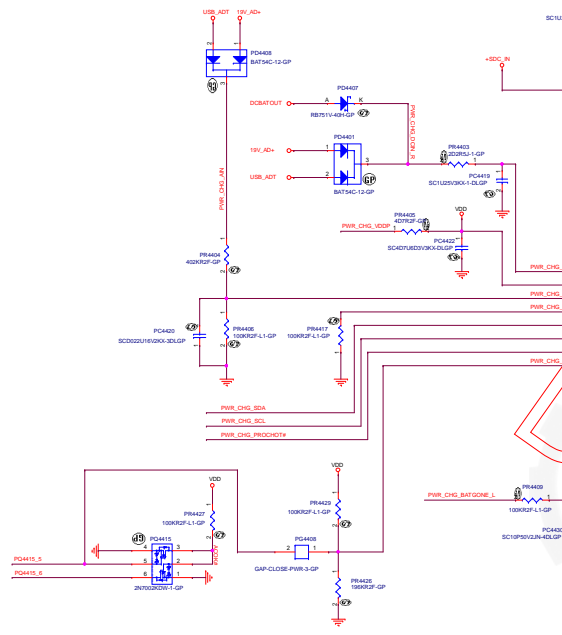
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Connected_Standby(2/2)			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 42 of	106

24 HW_ACAVRN_NB <<<—
24 PS_ID <<<—
17,44 AC_RWF >>>—
44 PBAT_CHG_SMBCLK <<<>>>—
44 PBAT_CHG_SMBDAT <<<>>>—
24,44 PBAT_PRES# <<<>>>—
24 AC_DIS >>>—





Vinafix.com



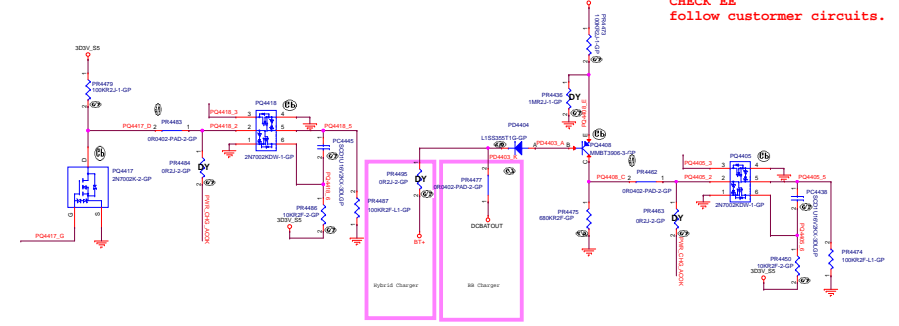
PROG-GND RESISTANCE (kΩ)				DEFAULT SWITCHING FREQUENCY		Autonomous charging		DEFAULT AC LimIt Res(A)	
MIN	TYP	1%	MAX	CELL #					
0				1	733kHz	No	No	0.476	
8.45					733kHz	No	No	1.5	
14.7					1MHz	No	No	1.5	
21.0					1MHz	No	No	0.476	
28.0					733kHz	Yes	Yes	0.476	
35.7					733kHz	Yes	Yes	1.5	
43.2				2	733kHz	Yes	Yes	0.476	
52.3					733kHz	Yes	Yes	0.476	
61.9					1MHz	No	No	0.476	
71.5					1MHz	No	No	1.5	
82.5					733kHz	No	No	1.5	
93.1					733kHz	No	No	0.476	
105				3	733kHz	No	No	0.476	
118					733kHz	No	No	1.5	
133					1MHz	No	No	1.5	
147					1MHz	No	No	0.476	
162					733kHz	Yes	Yes	0.476	
178					733kHz	Yes	Yes	1.5	
196				4	733kHz	Yes	Yes	0.476	
215					733kHz	Yes	Yes	0.476	
237					1MHz	No	No	0.476	
261					1MHz	No	No	1.5	
287					733kHz	No	No	1.5	
316					733kHz	No	No	0.476	
348				1	733kHz	No	No	0.476	

75_87333.071 CSD87330
IS = 100µA
Vgs = 5V
Id = 15A
Rds(on) = 9.45mΩ
Ls = 1.5nH
Vgs = 5V
Id = 15A
Rds(on) = 3.6mΩ

Need EE Check

Follow customer circuits.

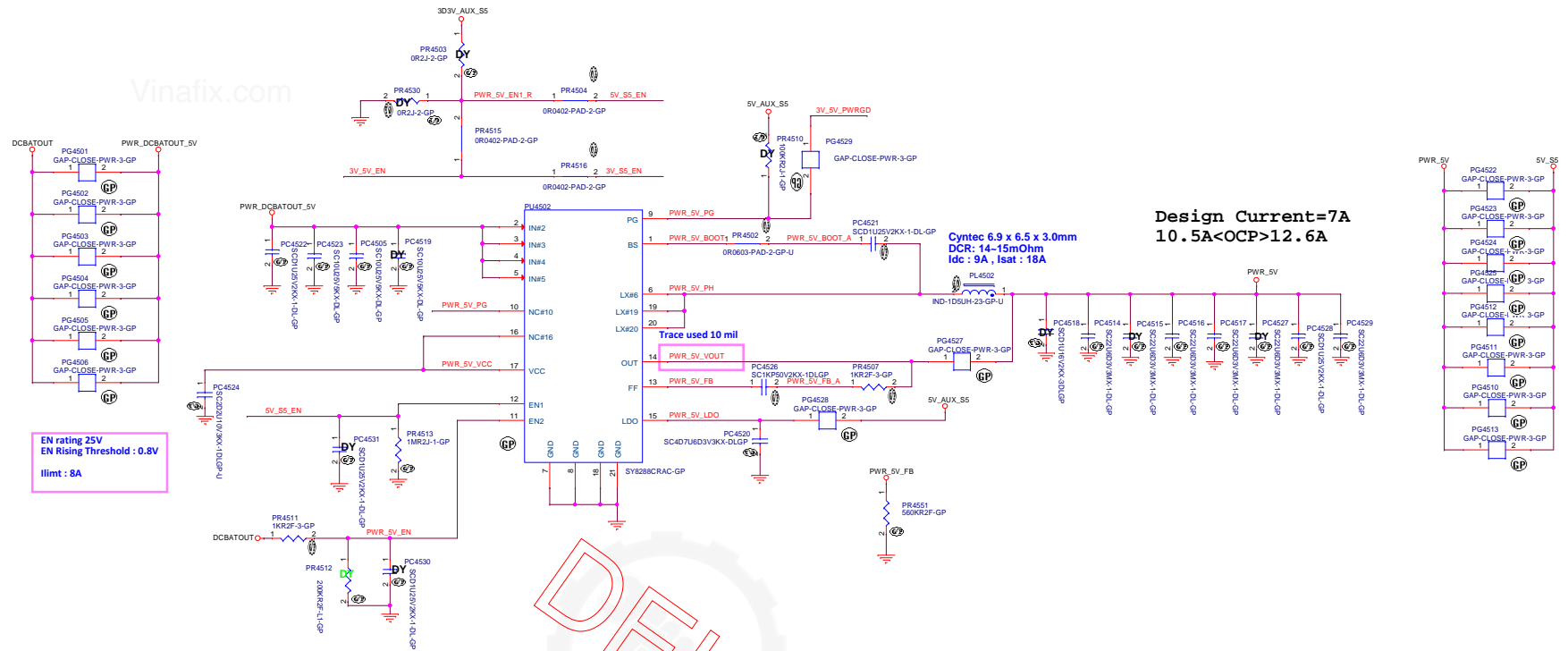
CHECK EE follow customer circuits.



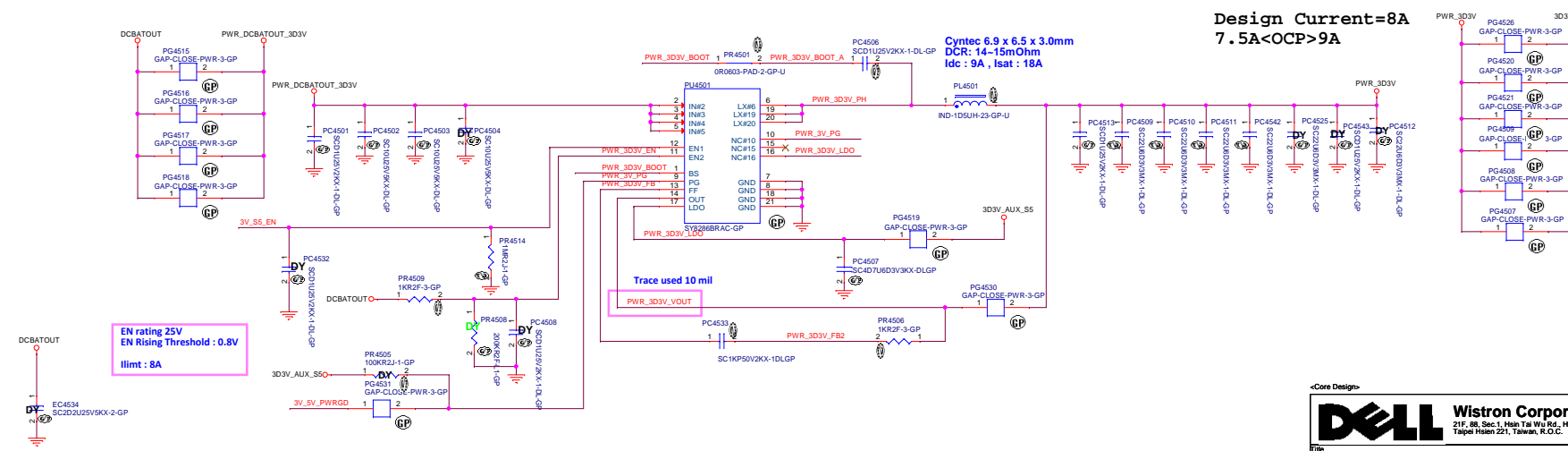
Main Func = PWR.Plane.Regulator_5V

Vinafix.com

40 3V_SS_EN >>>
17,25,40 3V_SS_PWRGD

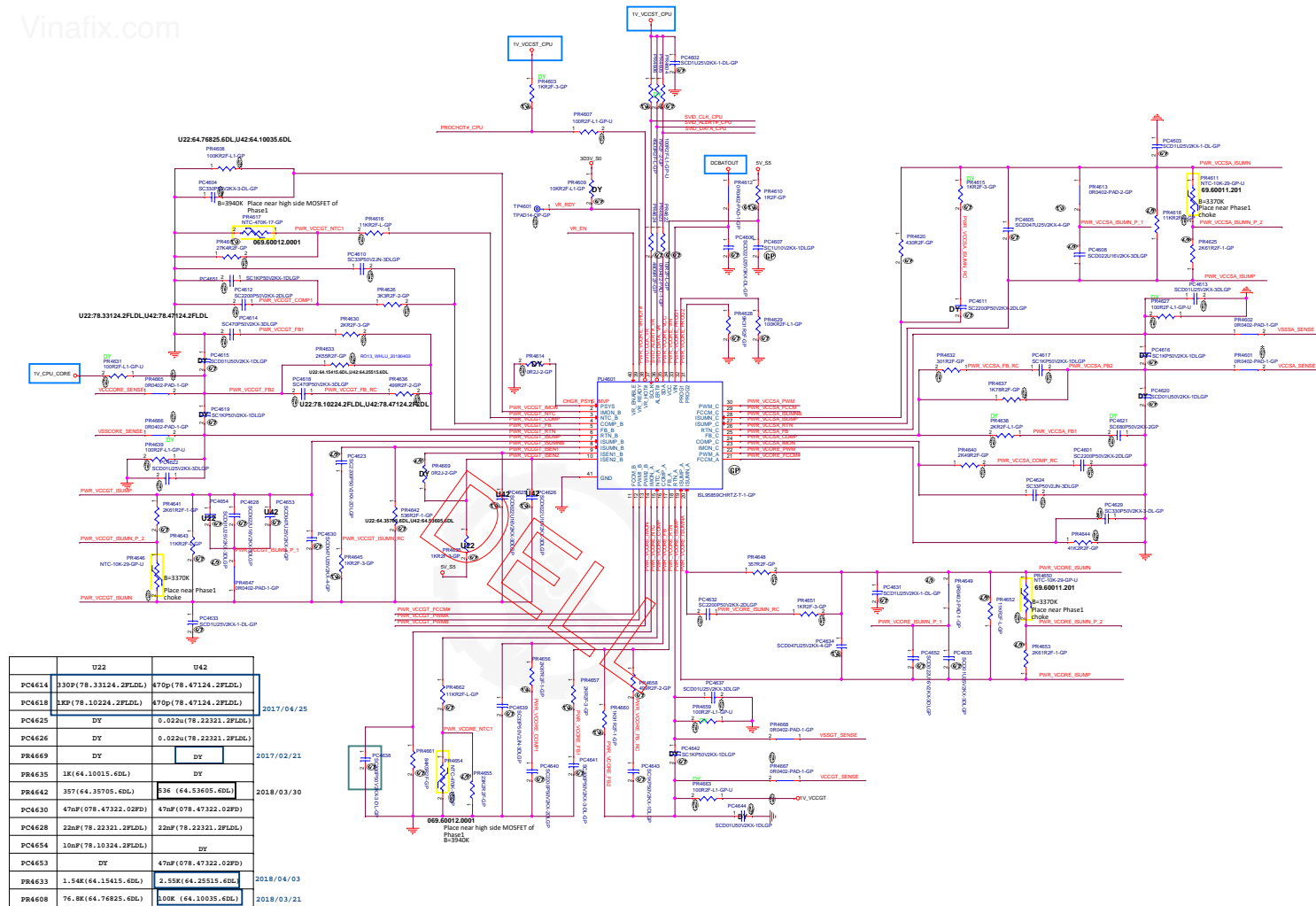


Main Func = PWR.Plane.Regulator_3D3V



<Core Design>


Vinafix.com



©Core Design

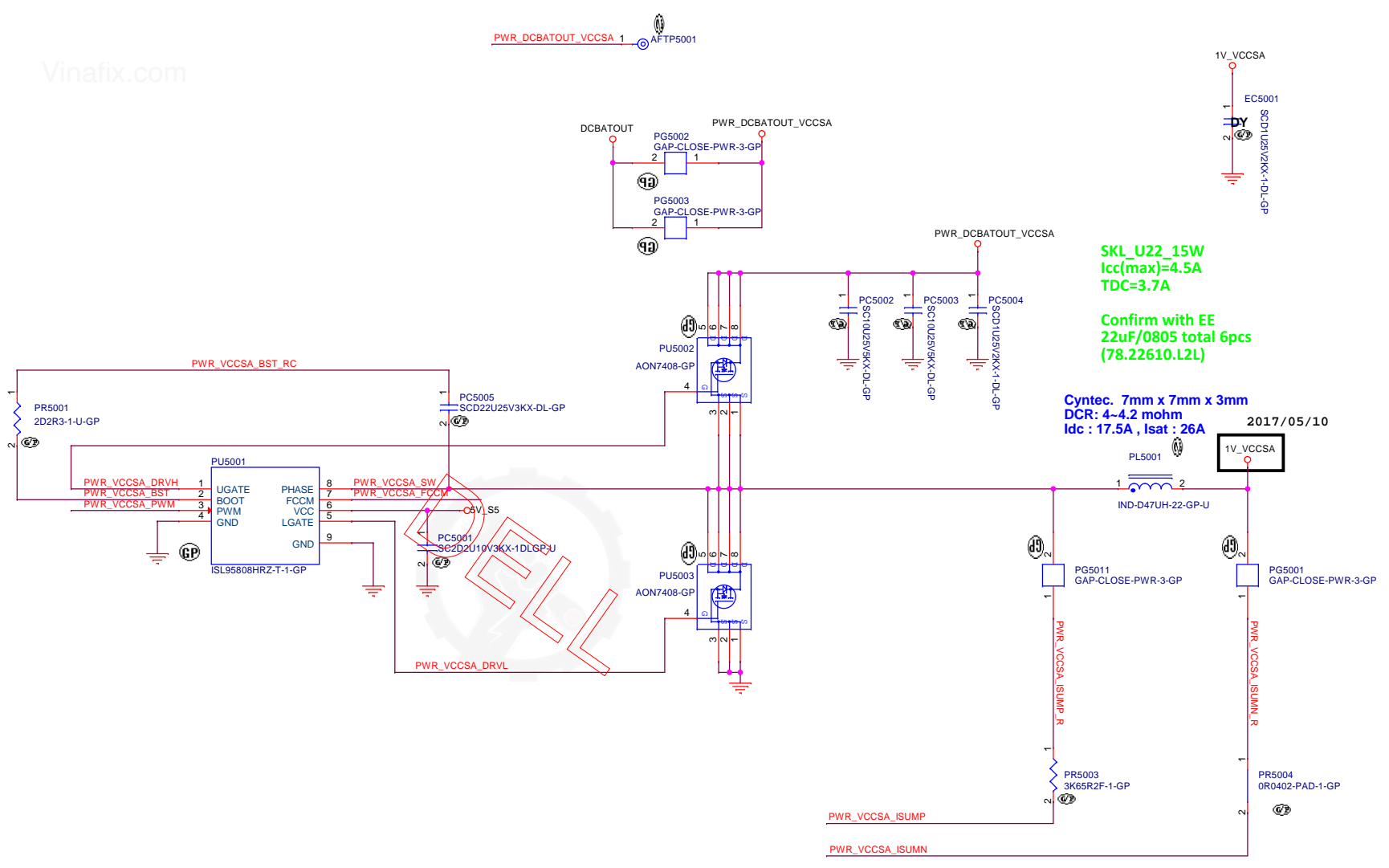
(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number RogueOne 13"	Rev SC
Date: Thursday, August 02, 2018		Sheet 49 of 106

Main Func = CPU_CORE

Vinafix.com



SKL_U22_15W
Icc(max)=4.5A
TDC=3.7A

Confirm with EE
22uF/0805 total 6pcs
(78.22610.L2L)

Cyntec. 7mm x 7mm x 3mm
DCR: 4~4.2 mohm
I_{dc} : 17.5A , I_{sat} : 26A
2017/05/10

Vinafix.com

(Blanking)



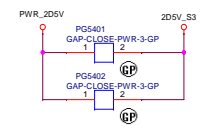
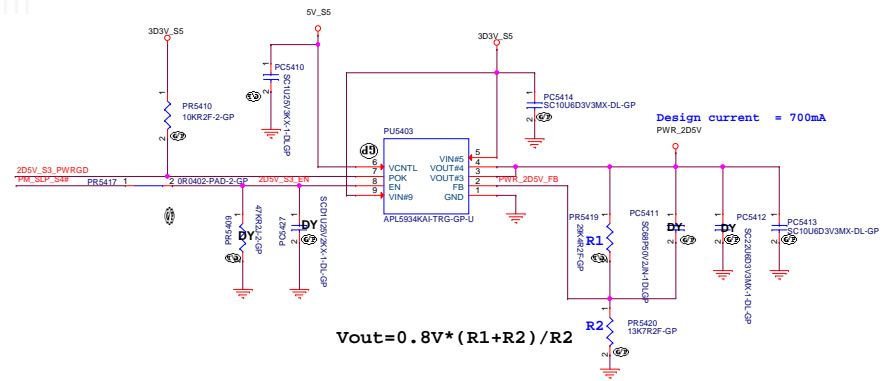
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 53 of	106

Vinafix.com

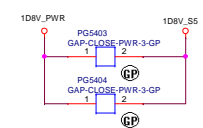
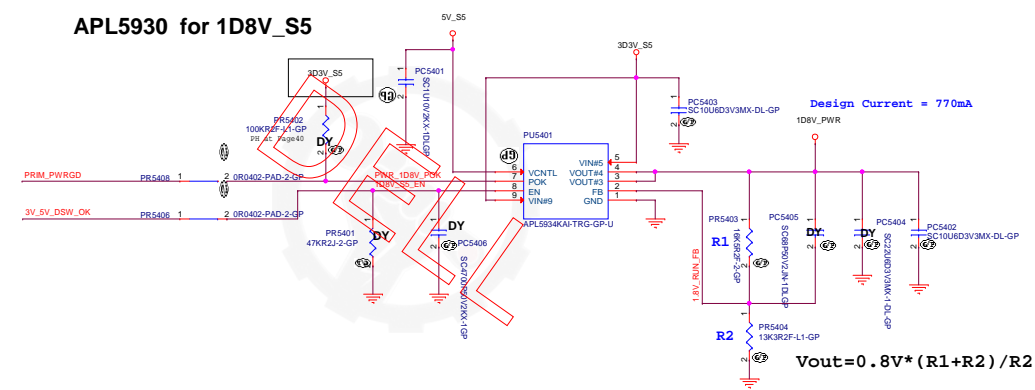
APL5930 for 2D5V

51 2D5V_S3_PWRGD
17.40.92 PM_SLP_S4#



APL5930 for 1D8V_S5

24.40 PRIM_PWRGD
25.52 3V_SV_DSW_OK

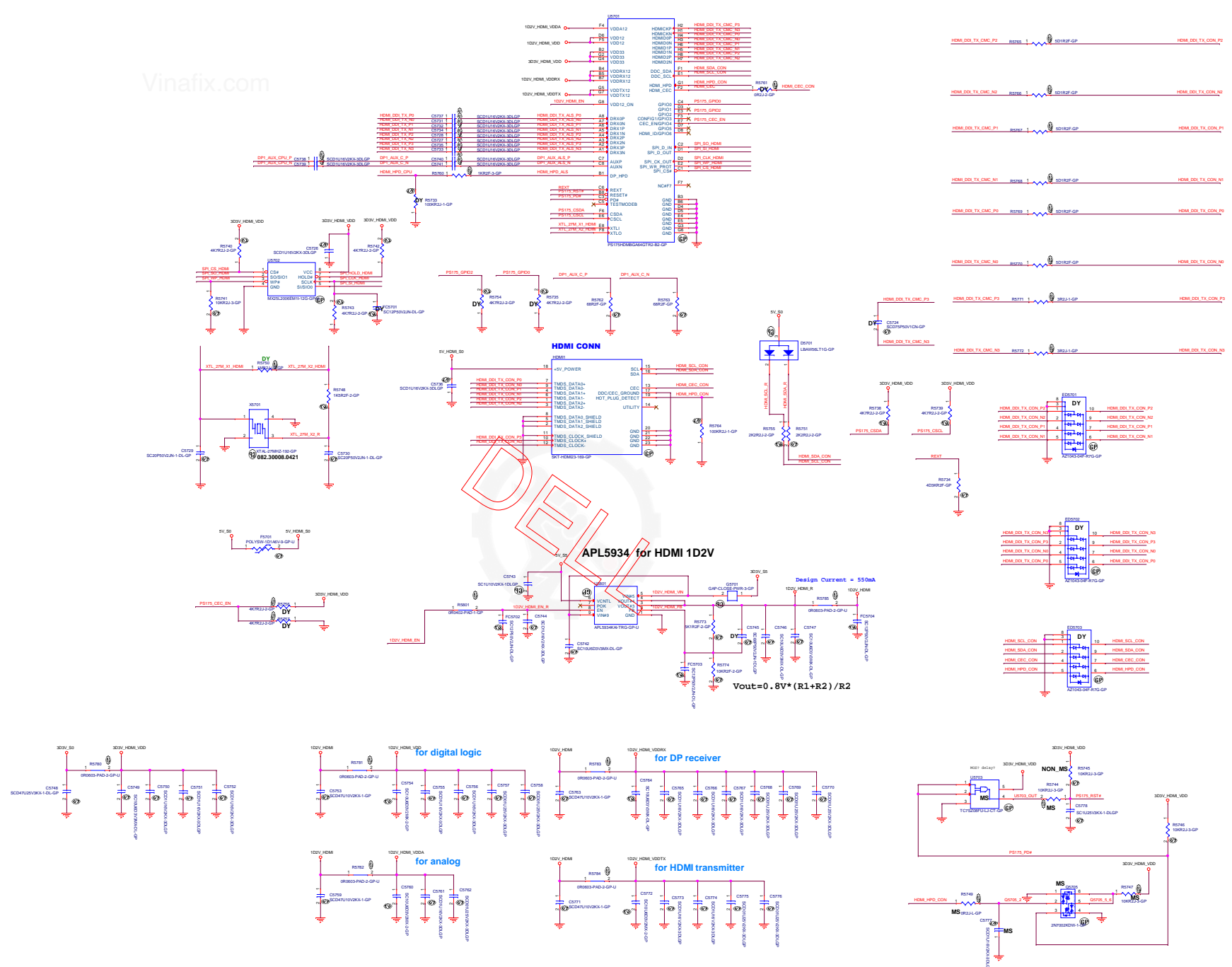


Vinafix.com

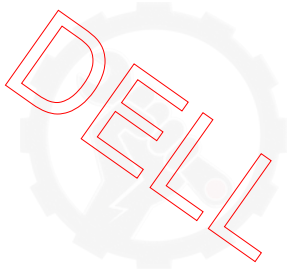
(Blanking)

<Core Design>

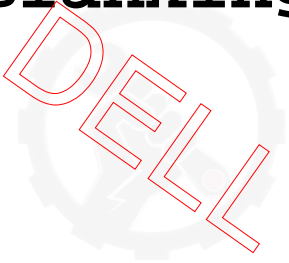
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 56 of	106



Vinafix.com



(Blanking)



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number RogueOne 13"		Rev
Date: Thursday, August 02, 2018		Sheet 59 of	106



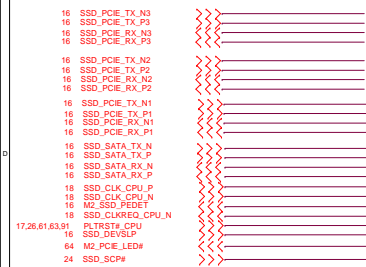
(Blanking)



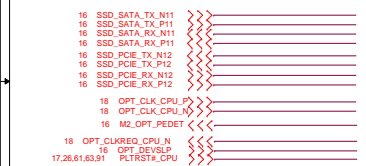
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 62 of	106

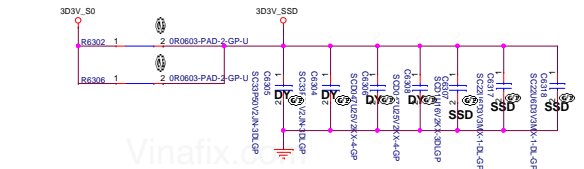
Main Func = SSD M.2



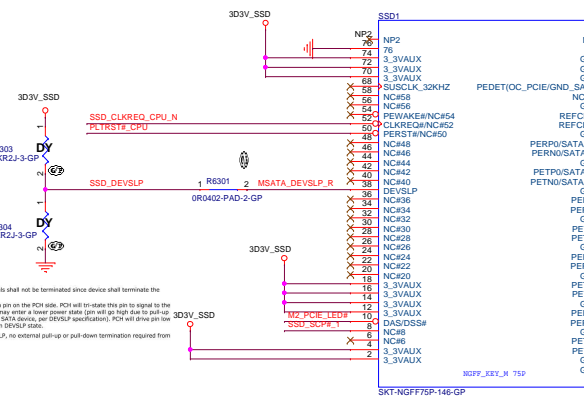
16 SSD_PCIE_TX_N3
16 SSD_PCIE_TX_P3
16 SSD_PCIE_RX_N3
16 SSD_PCIE_RX_P3
16 SSD_PCIE_TX_N2
16 SSD_PCIE_TX_P2
16 SSD_PCIE_RX_N2
16 SSD_PCIE_RX_P2
16 SSD_PCIE_TX_N1
16 SSD_PCIE_TX_P1
16 SSD_PCIE_RX_N1
16 SSD_PCIE_RX_P1
16 SSD_SATA_TX_N
16 SSD_SATA_TX_P
16 SSD_SATA_RX_N
16 SSD_SATA_RX_P
16 SSD_CLK_CPU_P
16 SSD_CLK_CPU_N
16 SSD_CLKREQ_CPU_N
16 SSD_DEVSPLP
64 M2_PCIE_LEDN
24 SSD_SCPN



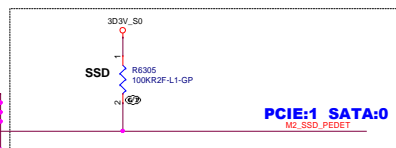
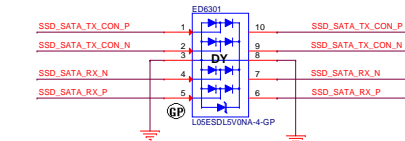
16 SSD_SATA_TX_N11
16 SSD_SATA_TX_P11
16 SSD_SATA_RX_N11
16 SSD_SATA_RX_P11
16 SSD_PCIE_TX_N12
16 SSD_PCIE_TX_P12
16 SSD_PCIE_RX_N12
16 SSD_PCIE_RX_P12
16 OPT_CLK_CPU_P
16 OPT_CLK_CPU_N
16 M2_OPT_PEDET
16 OPT_CLKREQ_CPU_N
16 OPT_DEVSPLP
17,26,61,63,61 PLTRSTF_CPU



SSD M.2 CONN

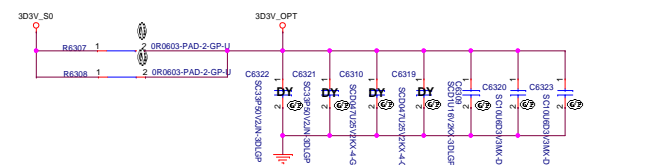


Important! SATA Host DEVSPLP signal:
• This is an open-drain pin on the PCI side. PCI will drive this pin to signal to the SATA device the SATA device, per DEVSPLP application. PCI will drive pin low to signal an error (DR00P state).
• When used as DEVSPLP, no external pull-up or pull-down termination required from SATA Host DEVSPLP.



PCIe:1 SATA:0 M2 SSD PEDET

2ND M.2



2ND M.2 CONN

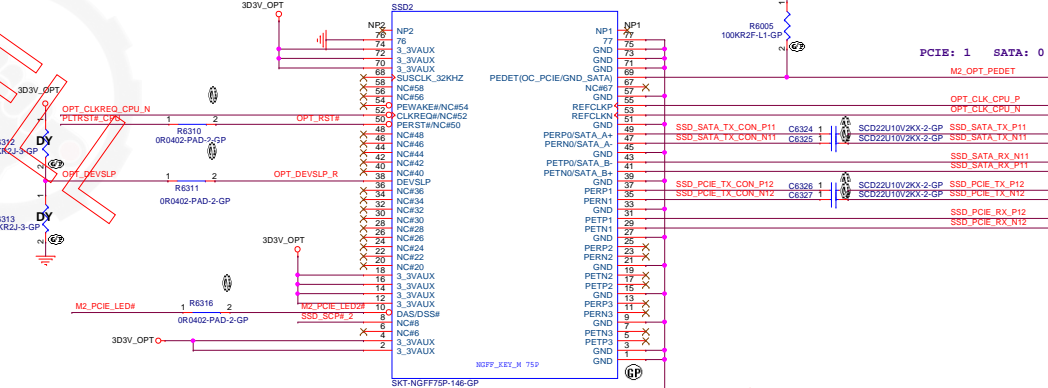
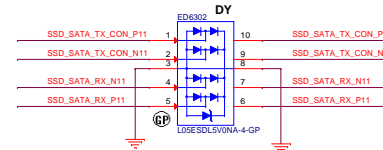


Table 13-11.SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:
1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* Gen 2 devices or PCIe* Gen3 devices, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48: Socket 3 SSD Pin-Out (Mechanical Key M) On Platform



<Core Design>



Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehchu,
Taipei Hsien 221, Taiwan, R.O.C.

(Reserved)

File

Size	Document Number	Rev
A2	RogueOne 13"	SC

Date: Thursday, August 02, 2018 Sheet 83 of 106

Main Func = Power BTN

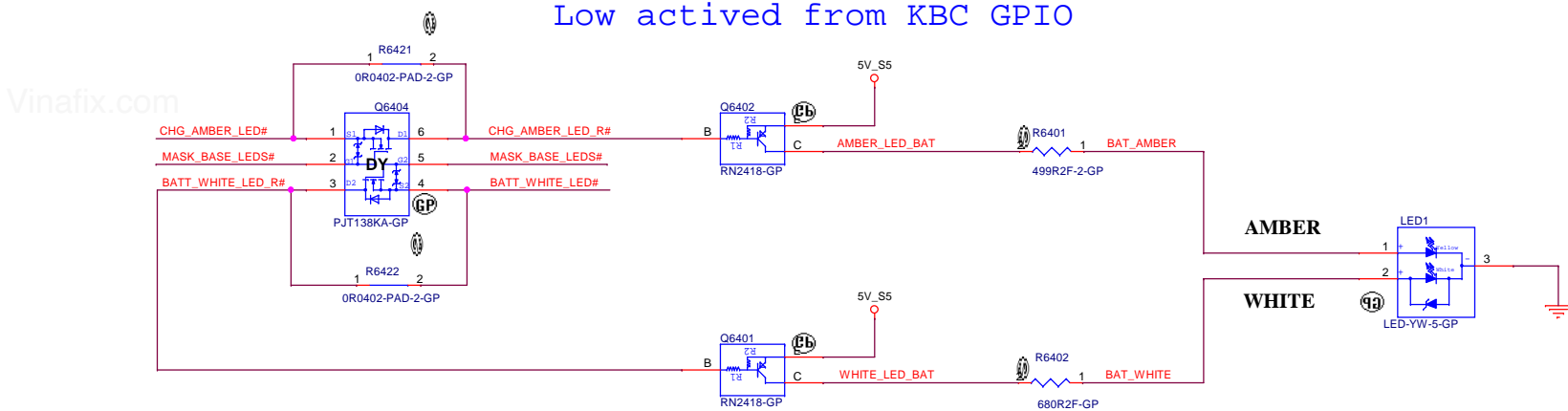
Battery LED1 (AMBER_LED)
Low activated from KBC GPIO

24 CHG_AMBER_LED# >>>—
24 BATT_WHITE_LED# >>>—

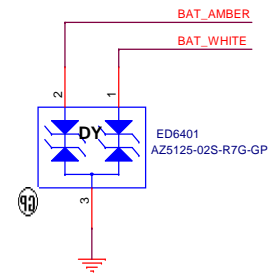
24 SYS_LED_MASK#_R >>>—
16 PCH_SATA_LED# >>>—
63 M2_PCIE_LED# >>>—

24,66,92 LID_CL_SIO# >>>—

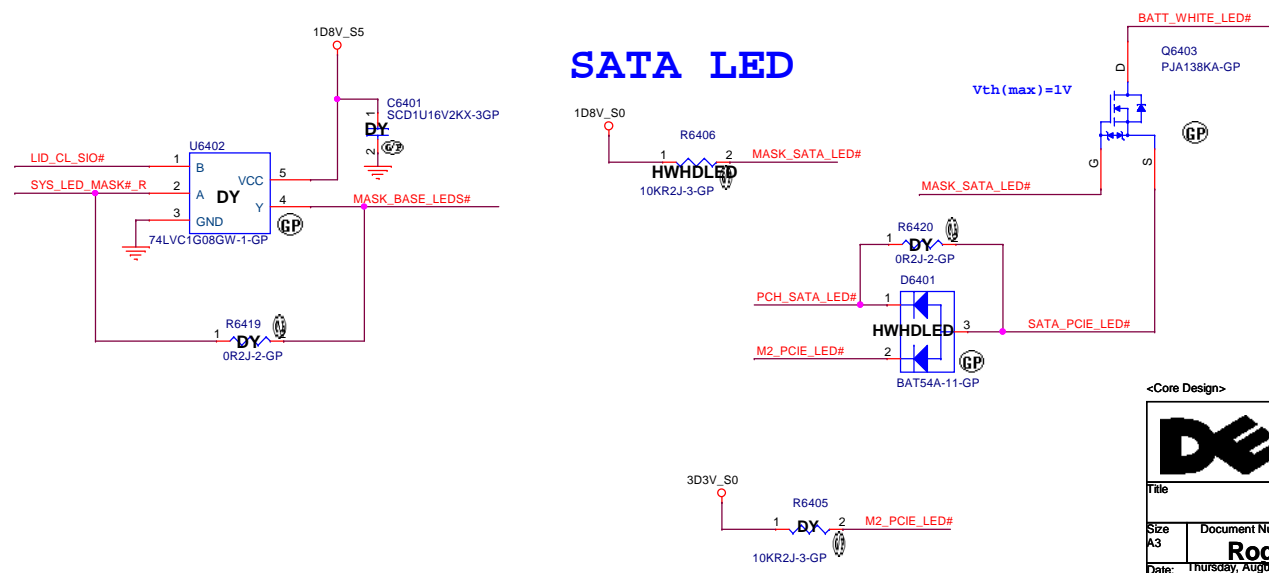
24 MASK_SATA_LED# >>>—

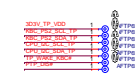


Battery LED2 (WHITE_LED)
Low activated from KBC GPIO



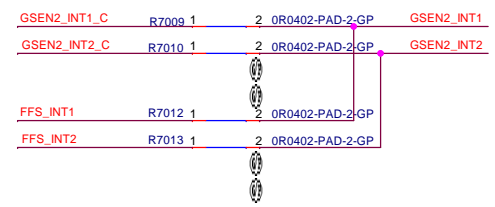
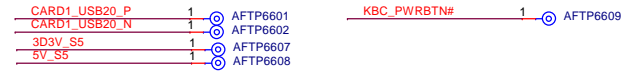
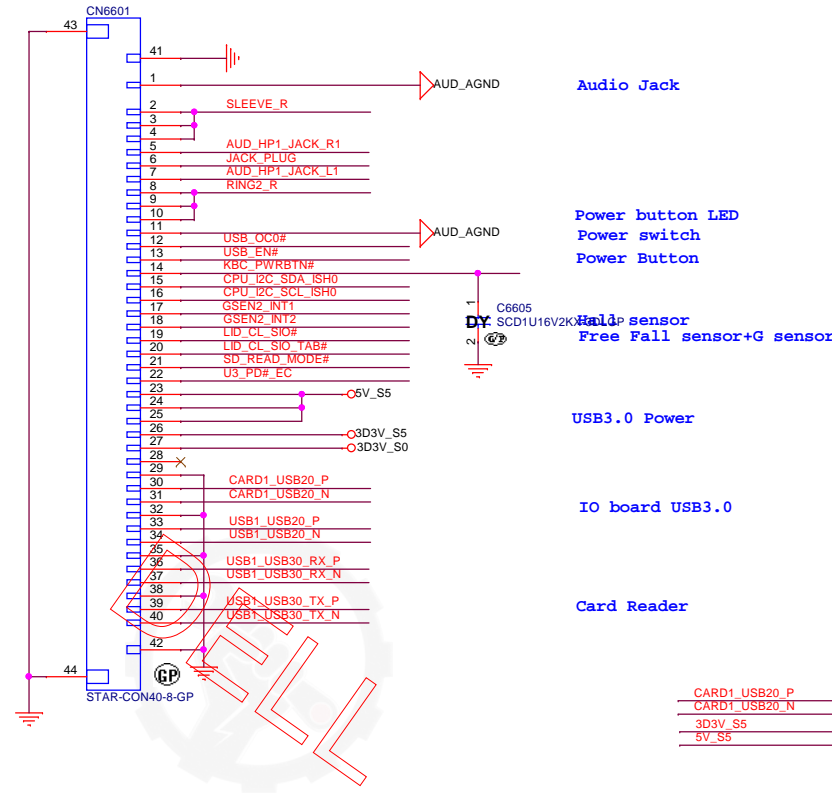
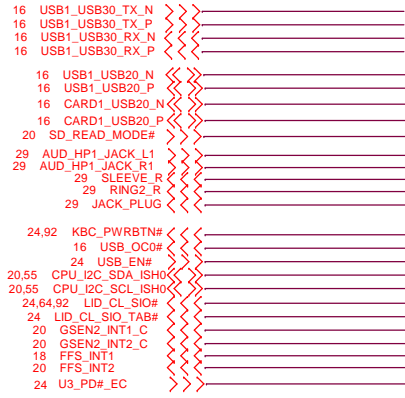
SATA LED



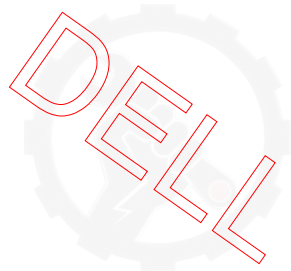


Main Func = IO Connector

Vinafix.com



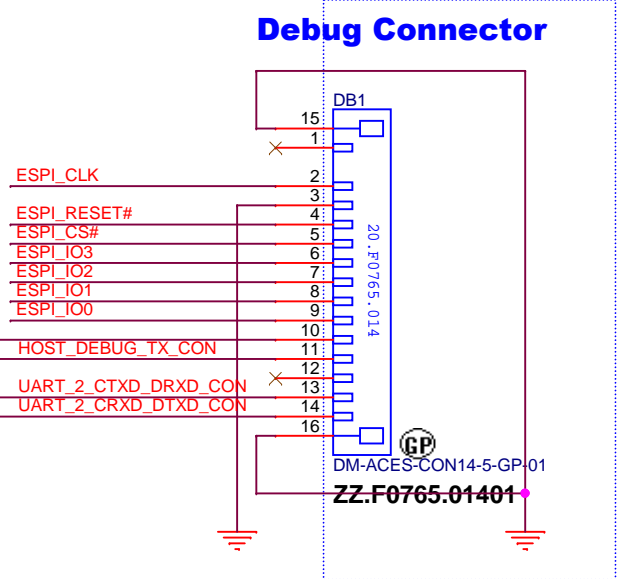
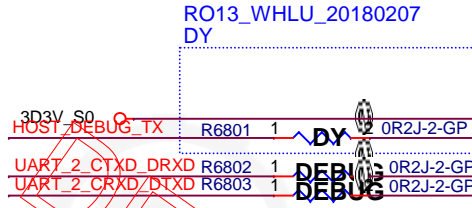
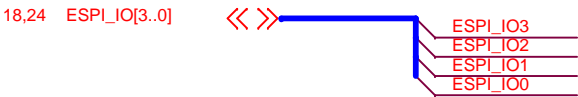
(Blanking)



<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 67 of	106

Main Func = Debug




DM-ACES-CON14-5-GP-01

ZZ.F0765.01401

RO13_20170822
DUMMY PAD to CONNECTOR 20.F0765.014

RO13_A00_20180629
use ZZ.F0765.01401(dummy pad) for MP

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

SizeA4

Document Number

RevSC

Date: Thursday, August 02, 2018

Sheet 68 of 106

(Blanking)



<Core Design>

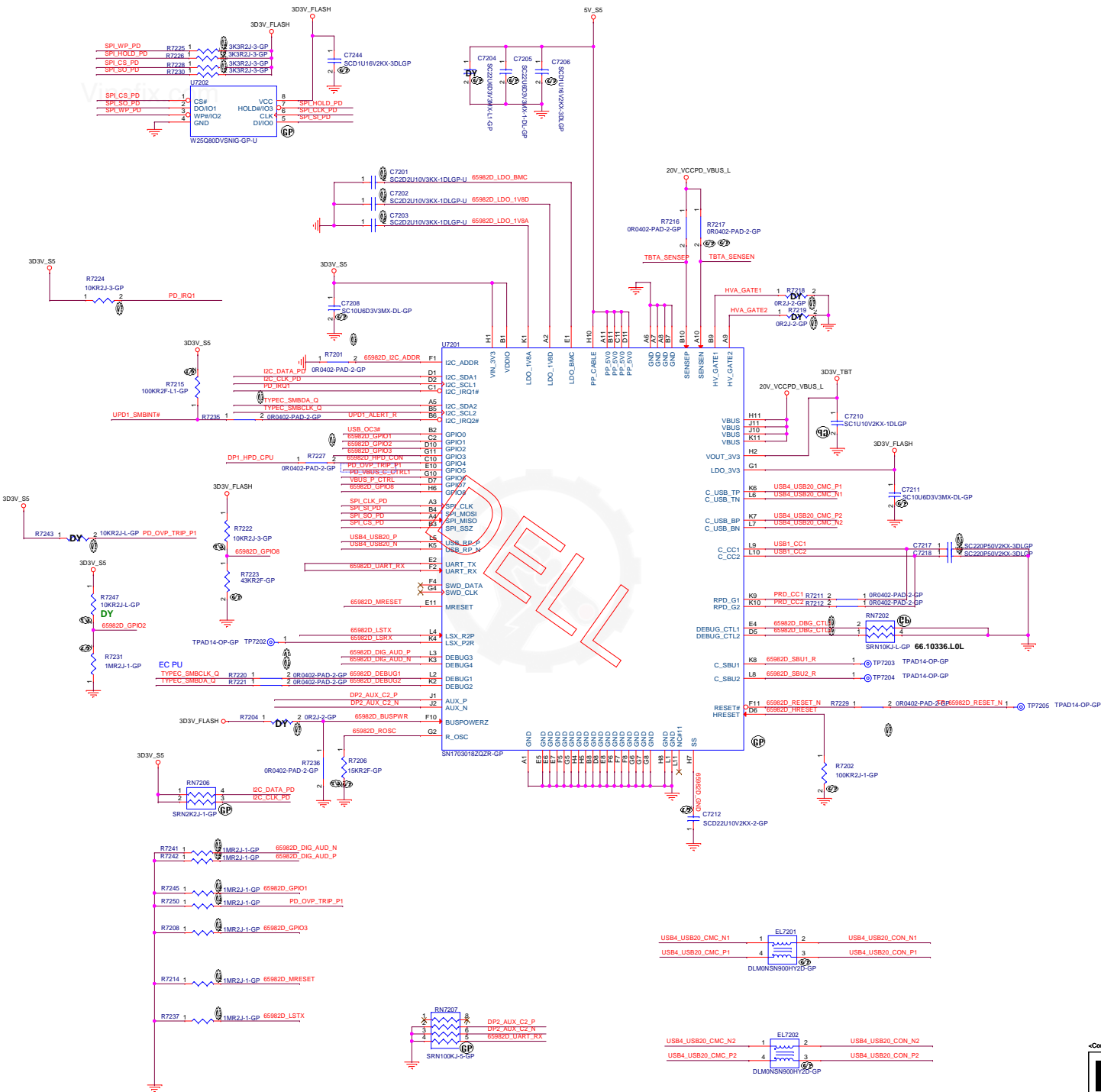
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number RogueOne 13"		Rev SC
Date: Thursday, August 02, 2018		Sheet 69 of	106

Vinafix.com

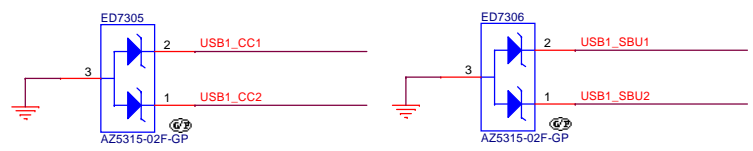
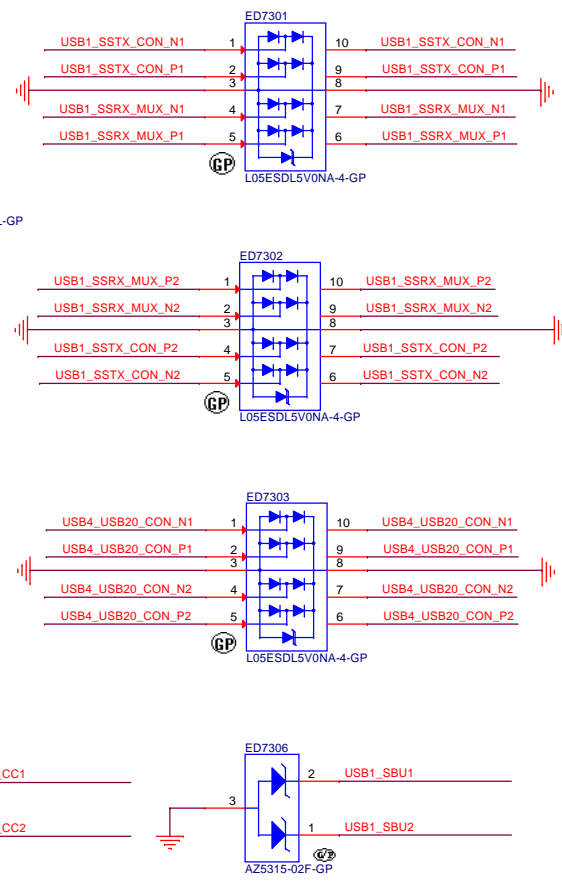
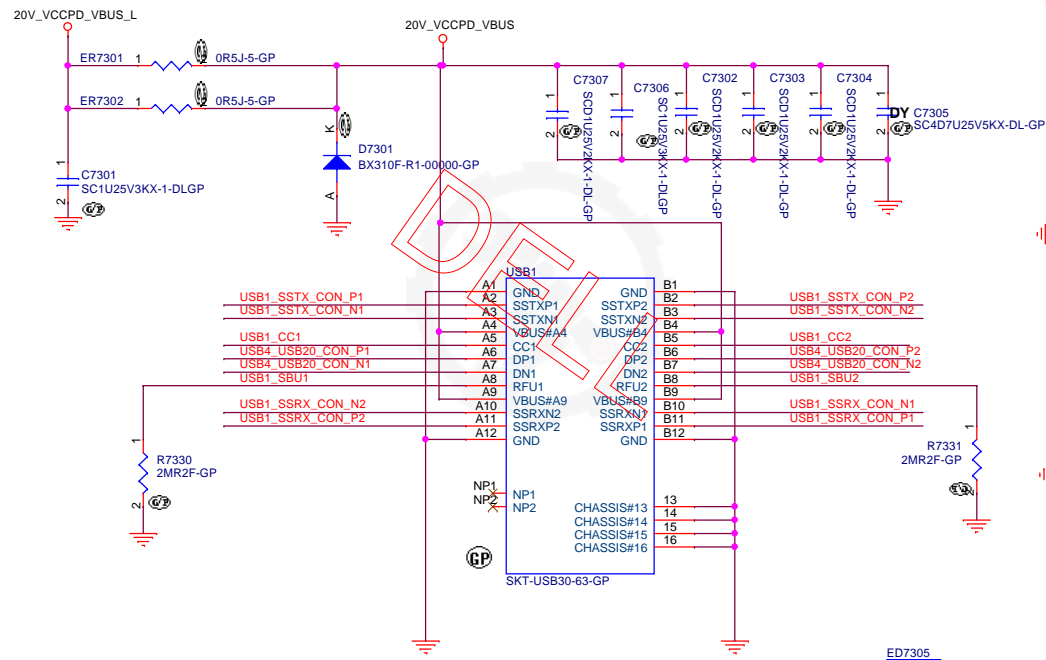
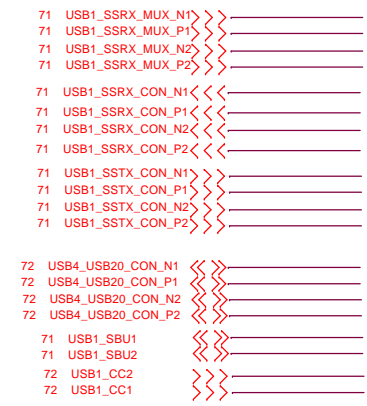


Main Func = TPS65982DC

- 4,71 DPI_HPD_CPU
- 74 PD_VBUS_C_CTRL1
- 16 USB_OC#
- 71 I2C_CLK_PD
- 71 I2C_DATA_PD
- 24 TYPEC_SMBDA_O
- 24 TYPEC_SMBCLK_O
- 24 UPD1_SMBINT#
- 73 USB1_CC1
- 73 USB1_CC2
- 73 USB4_USB20_CON_N1
- 73 USB4_USB20_CON_N2
- 73 USB4_USB20_CON_P1
- 16 USB4_USB20_P
- 16 USB4_USB20_N

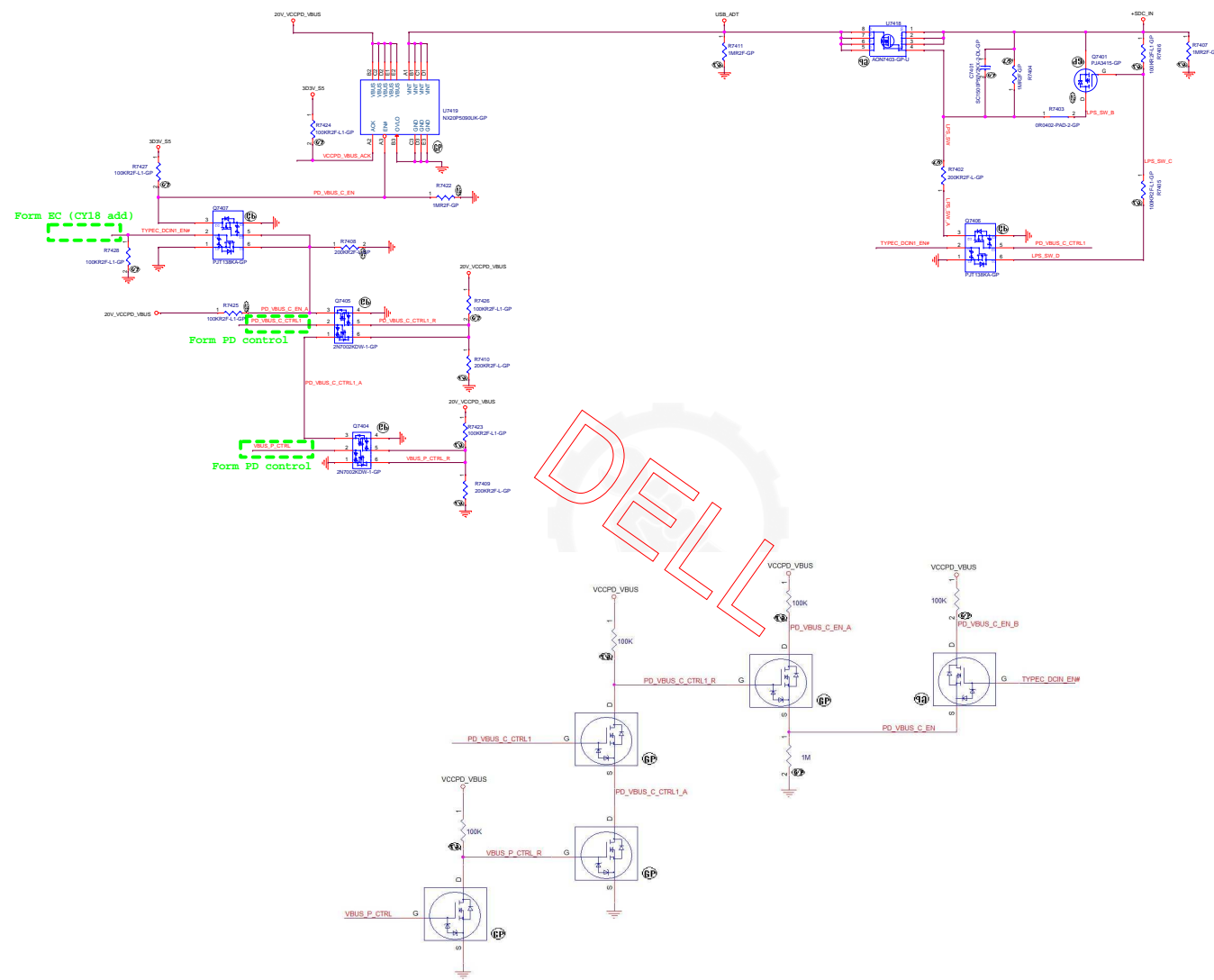


Main Func = TYPEC CONNECTOR



72 PD_VBUS_C_CTRL1 >>>
 24 TYPEC_DCHL_ENM >>>
 72 VBUS_P_CTRL >>>
 44 VCCPD_VBUS_ACK <<<

Vinafix.com



Vinafix.com



Main Func = dGPU


Vinafix.com



Vinafix.com




<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
GPU(5/5)PWR/GND		
Size	Document Number	Rev
Custom	RogueOne 13"	SC
Date	Thursday, August 02, 2018	Sheet 77 of 106






Vinafix.com



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU(55)PWR/GND

Size

Document Number

Rev

Custom

RogueOne 13"

SC

Date

Thursday, August 02, 2018

Sheet

80


of

106

Vinafix.com



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title		
GPU-VRAM1,2 (1/4)		
Size	Document Number	Rev
A3	RogueOne 13"	SC
Date: Thursday, August 02, 2018		
Sheet 81 of 106		


		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RT8812 VGACORE			
Size A2	Document Number	Rev	
	RogueOne 13"	SC	
Date: Thursday, August 02, 2018		Sheet 82	of 106

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
RT8812 VGACORE RogueOne 13"	
Size A2	Document Number <div style="text-align: right;">Rev SC</div>
Date: Thursday, August 02, 2018 Sheet 82 of 106	

Vinafix.com





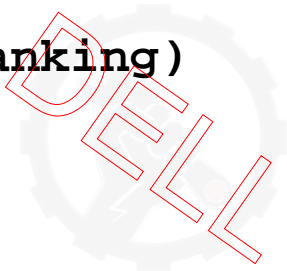
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM7,8 (4/4) RogueOne 13"			
Size A3	Document Number	Rev SC	
Date: Thursday, August 02, 2018	Sheet 84	of	106

Vinafix.com



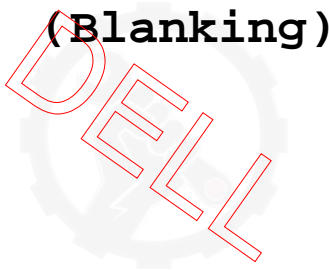
«Core Design»		 Wistron Corporation 21F, 88, Sec. 2, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU Discrete Power Size A2 Document Number RogueOne 13" Rev			
Date: Thursday, August 02, 2018 Sheet 86 of 106 SC			

(Blanking)

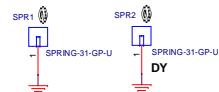


<Core Design>

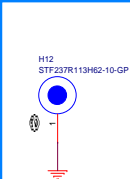
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A3	RogueOne 13"		SC
Date: Thursday, August 02, 2018		Sheet	87 of 106



34.4YW18.001

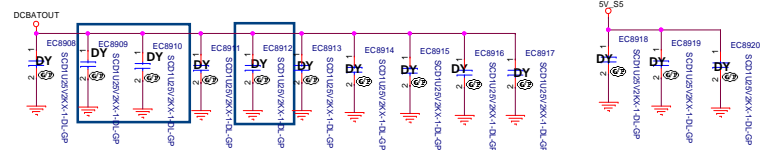


Type-C

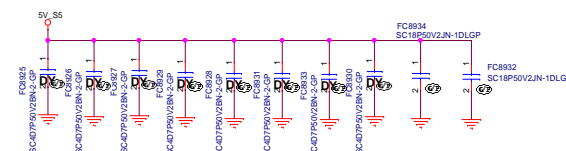
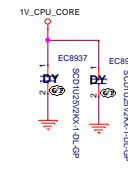
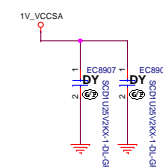
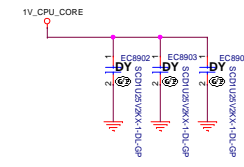
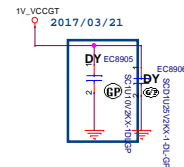
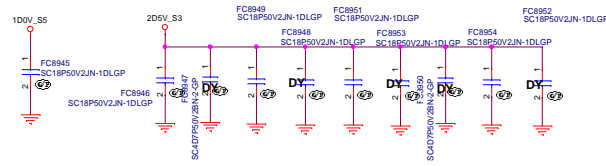
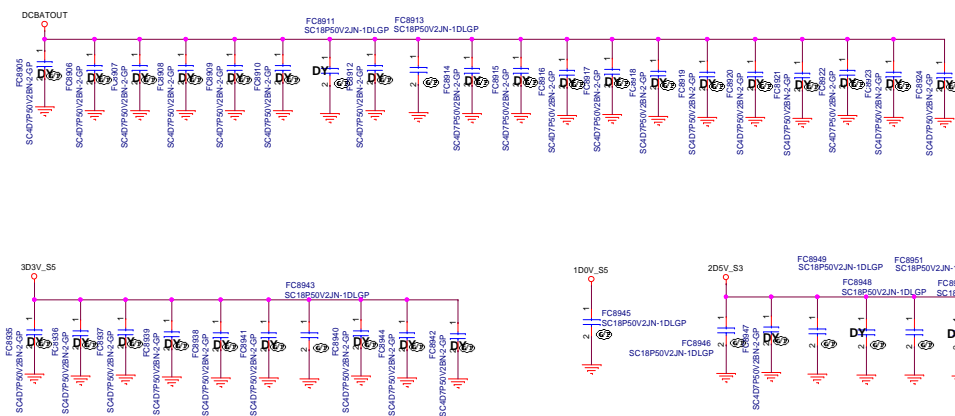


SSID = EMI

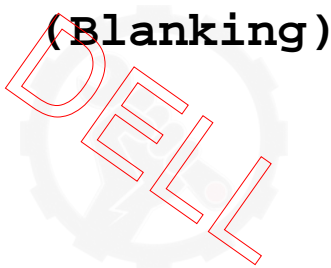
Mind the voltage rating of the caps.



SSID = RF



Vinafix.com

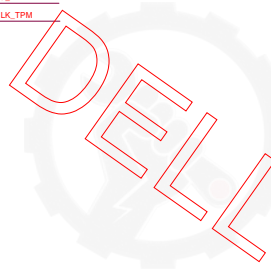
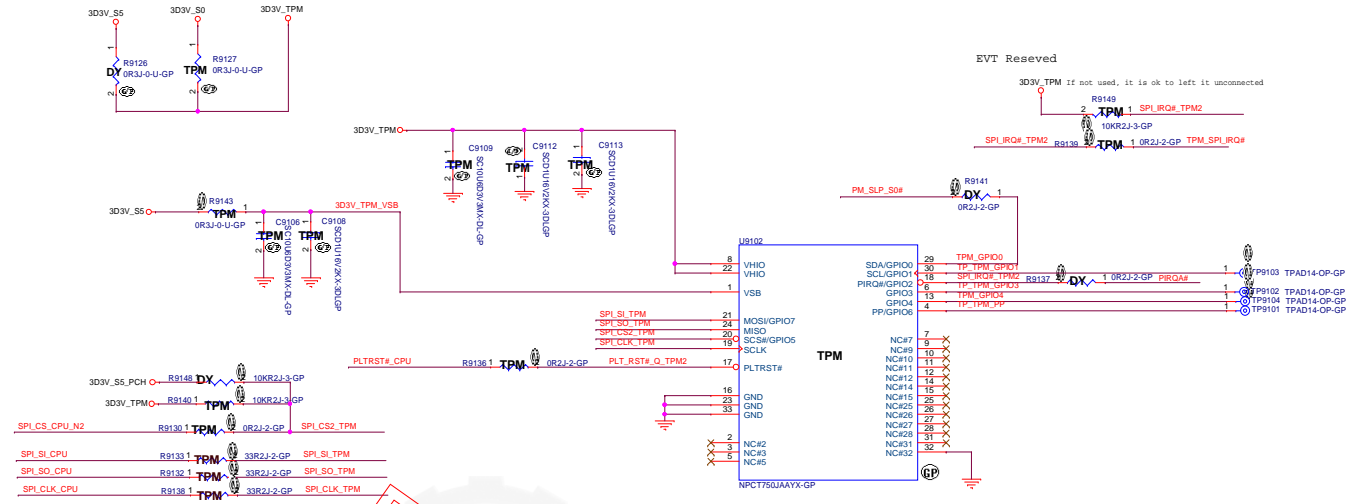


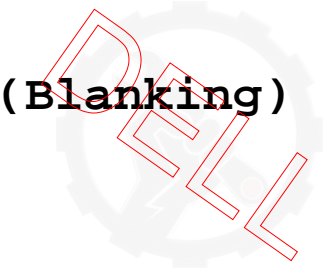
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A3	RogueOne 13"		SC
Date: Thursday, August 02, 2018		Sheet 90 of 106	1

Vinafix.com

20 PIRQ#
18 TPM_SPL_IRQ#
17,26,61,63 PLTRST#_CPU
17,24,40 PM_SLP_S0#
18 SPI_CS_CPU_N2
18,25 SPI_SO_CPU
15,18,25 SPI_SI_CPU
15,25 SPI_CLK_CPU





(Blanking)

Vinafix.com

(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			(Reserved)		
Size	Document Number				Rev
A3	RogueOne 13"				SC
Date: Thursday, August 02, 2018			Sheet	94 of 106	

Vinafix.com

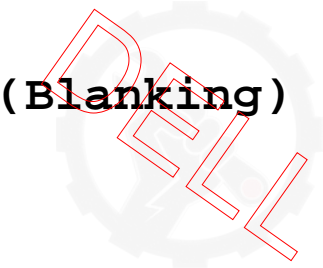
(Blanking)

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

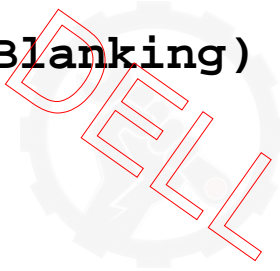
Title			(Reserved)		
Size	Document Number				Rev
A3	RogueOne 13"				SC
Date: Thursday, August 02, 2018			Sheet	95 of 106	



(Blanking)

Vinafix.com

(Blanking)



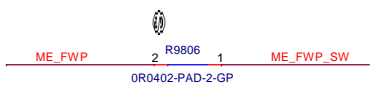
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LVDS Switch			
Size	Document Number		Rev
A3	RogueOne 13"		SC
Date:	Thursday, August 02, 2018		Sheet 97 of 106

Main Func = SWITCH

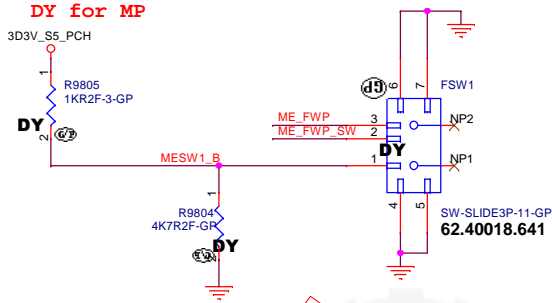
Vinafix.com

24 ME_FWP >>>
19 ME_FWP_SW <<<



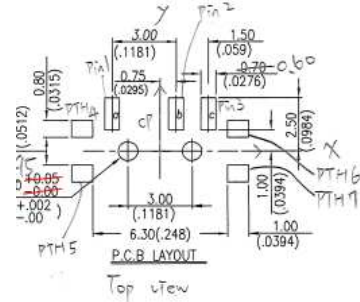
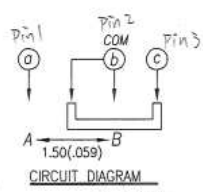
Firmware SW

Default setting:pull LOW
DY for MP



	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

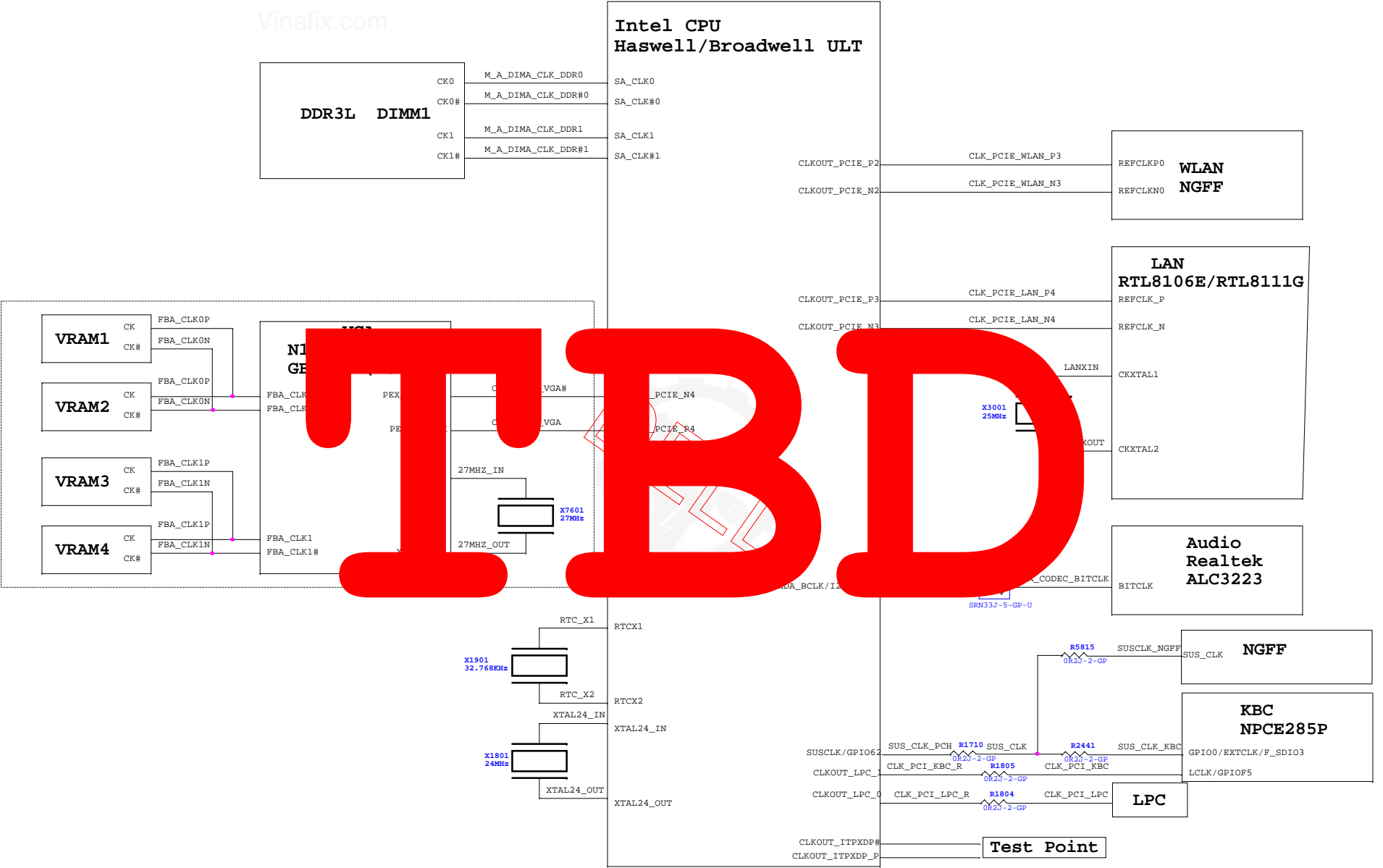
*Symbol same as
62.40018.641



SSID = Debug



CLK Block Diagram



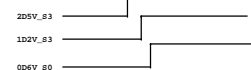
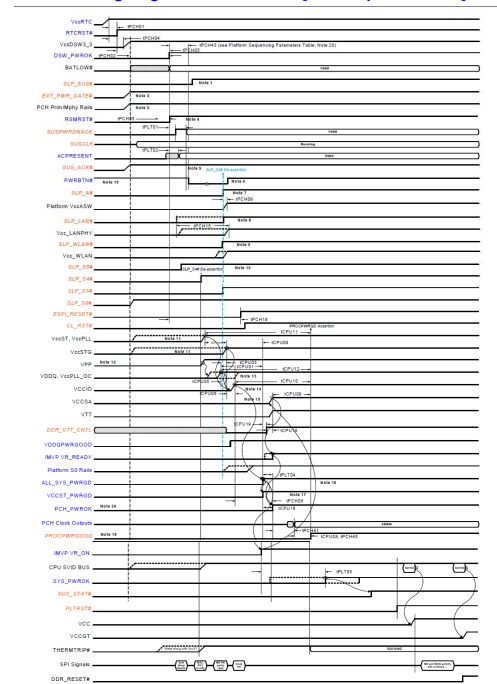
[illegible]

DELETED

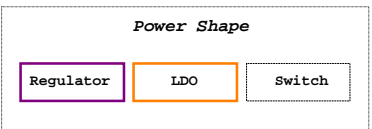
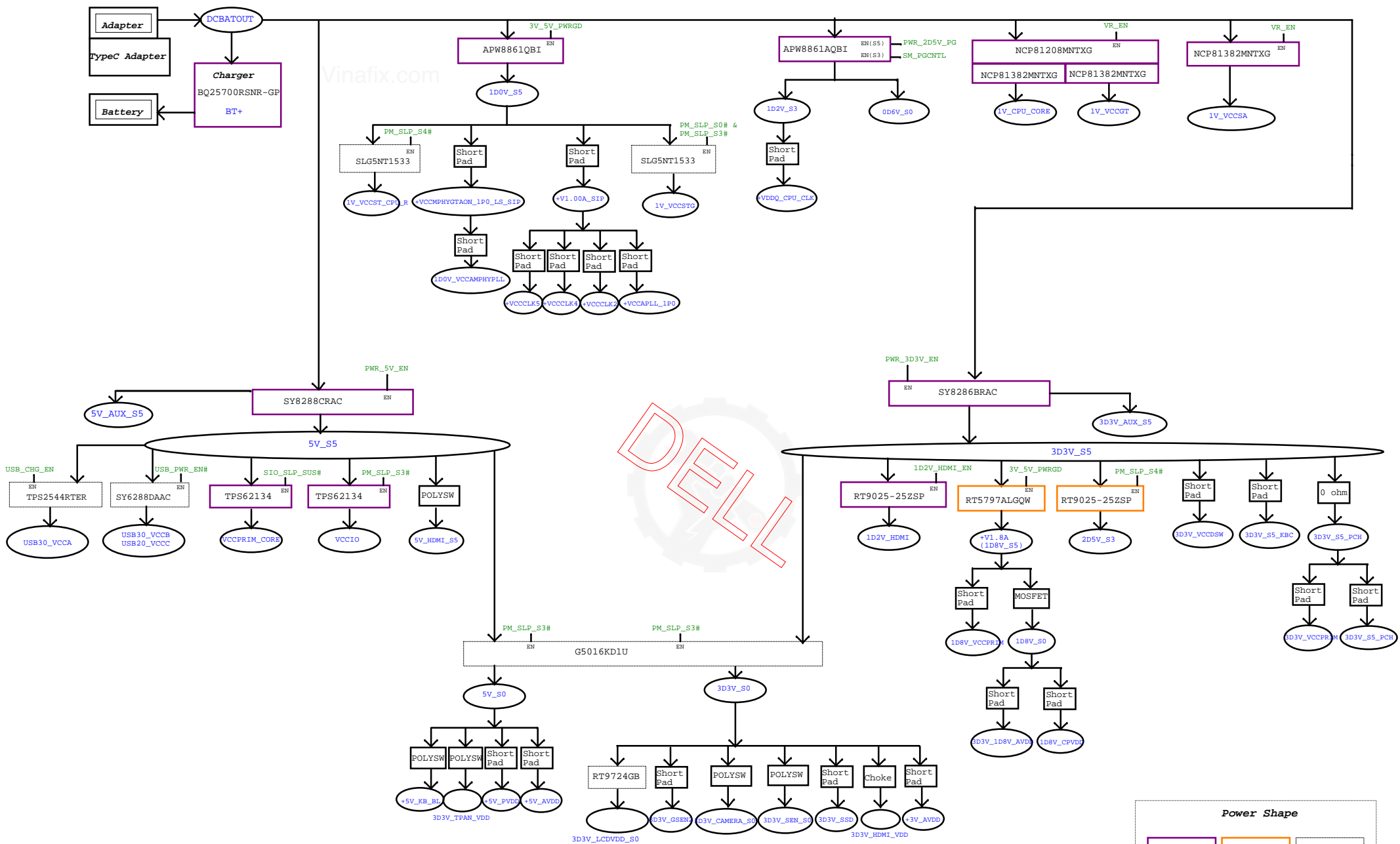


Sheet 101 of 106

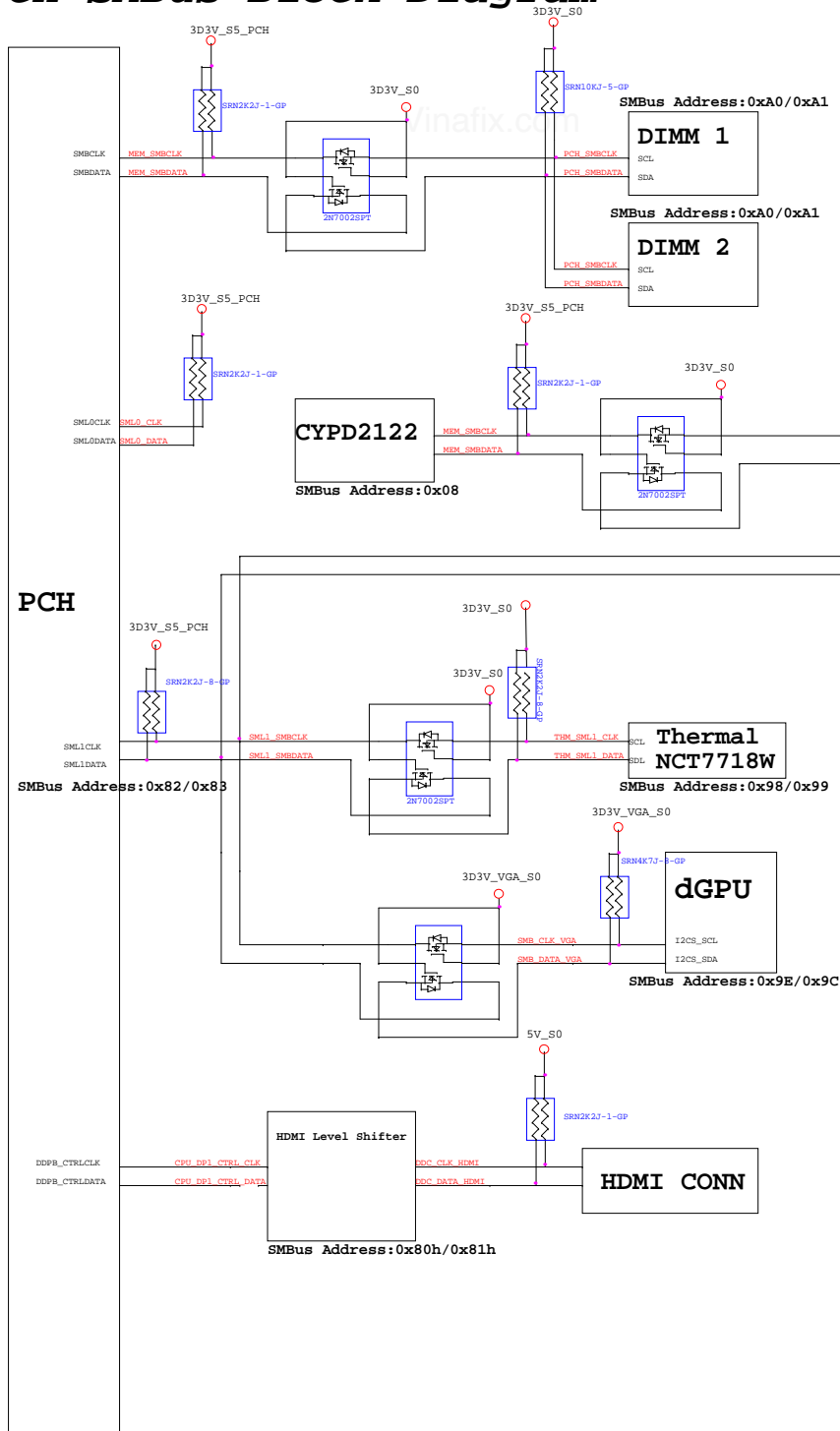
For DDR4 power sequence



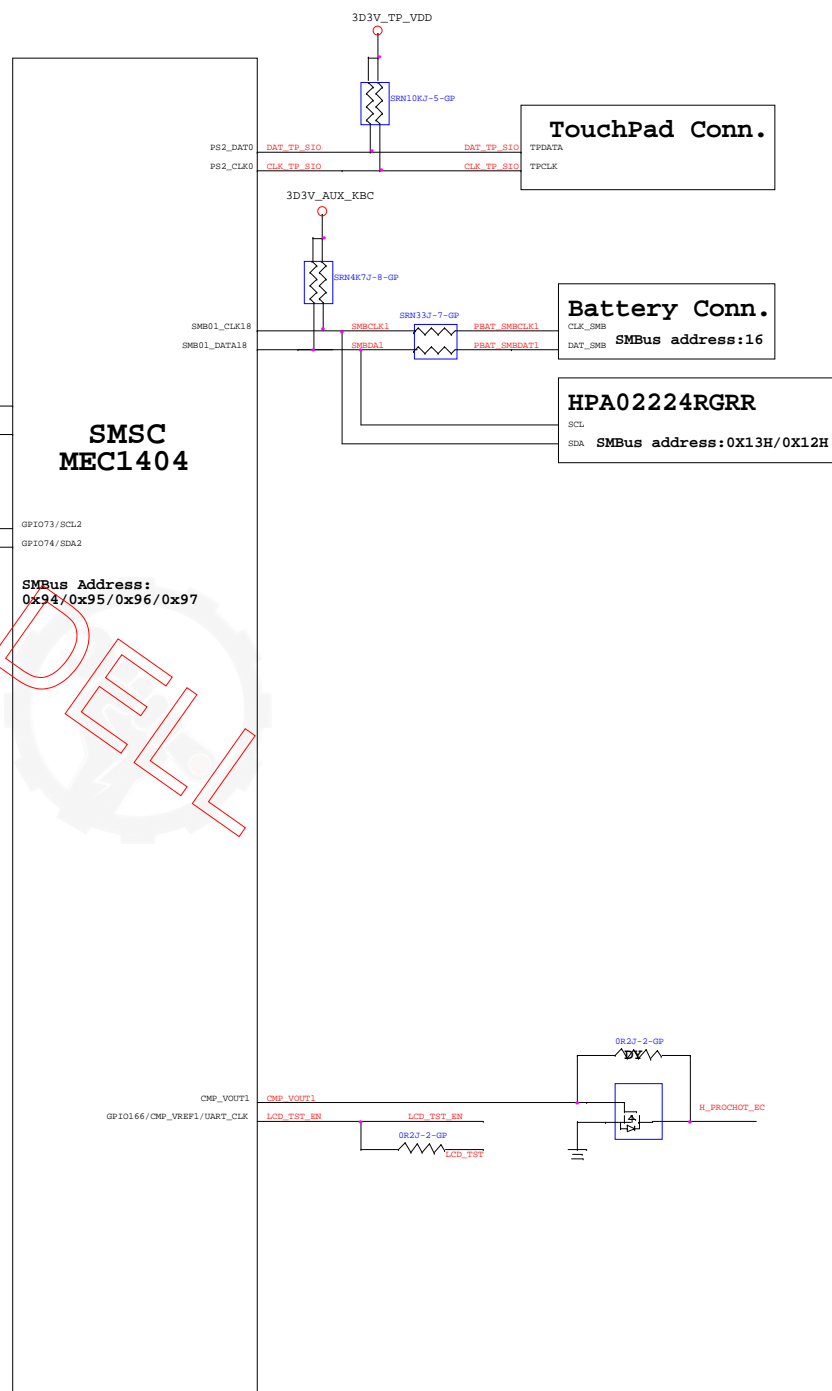
infix.com



PCH SMBus Block Diagram

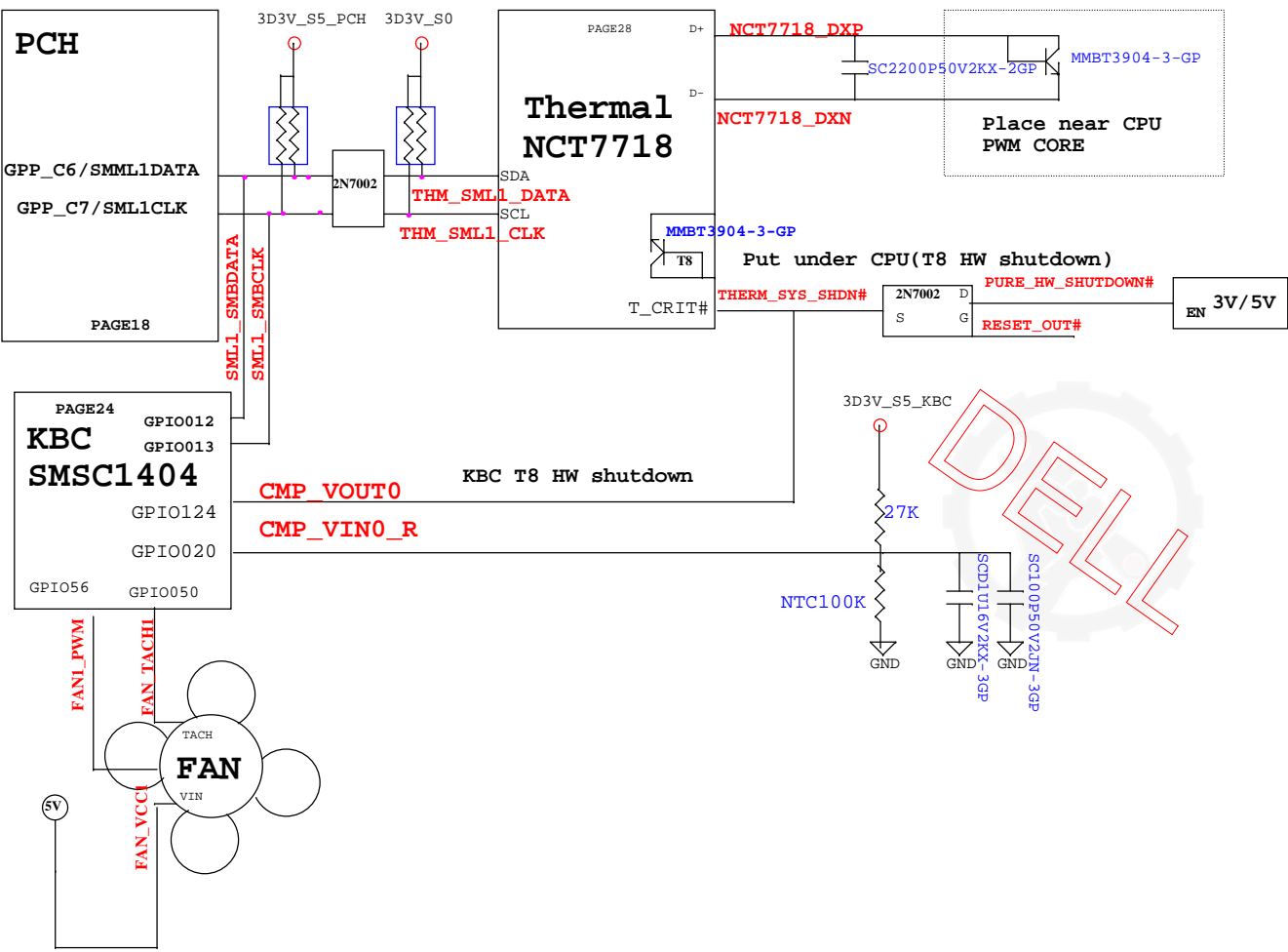


KBC SMBus Block Diagram

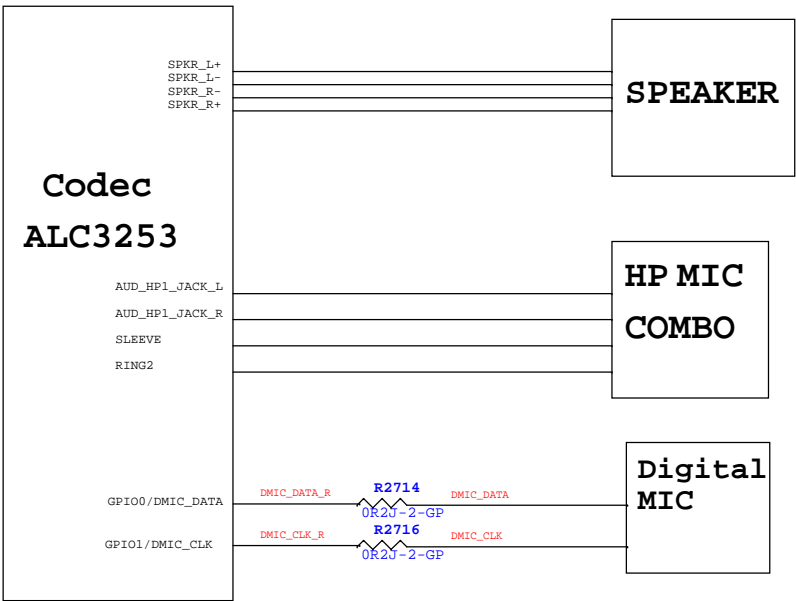


Thermal Block Diagram

Vinafix.com



Audio Block Diagram



<Core Design>

Vinafix.com



<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SIP connector

Size
A

Document Number

RogueOne 13"

Rev

SC

Date: Thursday, August 02, 2018

Sheet 106 of 106